

Compal Confidential

NAL90/NALG0 M/B Schematics Document

Intel Auburndale/Clarksville Processor with DDRIII + Ixex Peak-M

2009-10-20

REV:1.0

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Issued Date	2009/5/12	Deciphered Date	2010/04/15	Title	
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				Document Number	
				Rev	
Date: Friday, October 23, 2009				Sheet 1 of 60	

Customer

NALG0 M/B LA-5681P Schematic

1.0

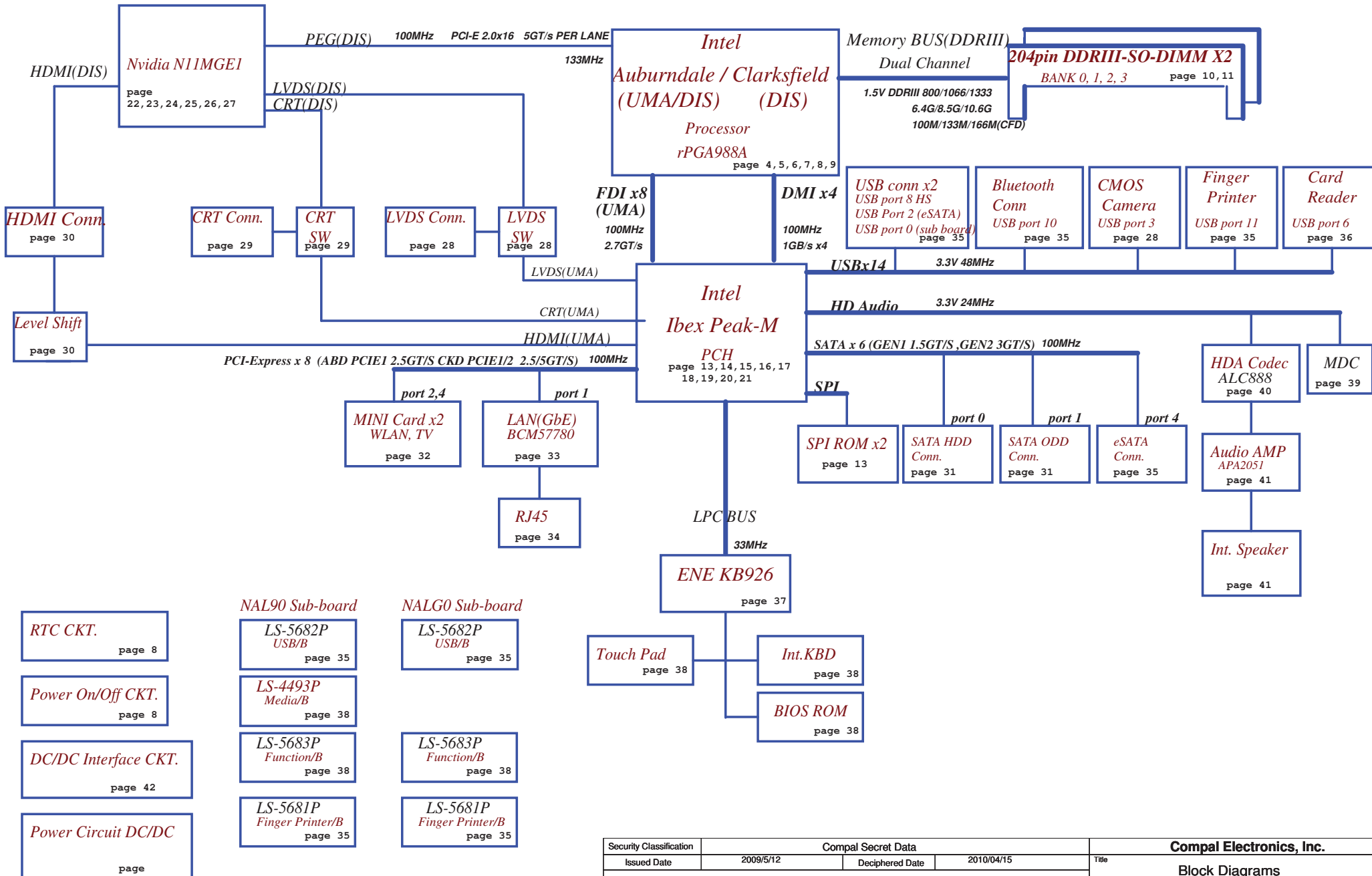
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Model Name NALG0

File Name : LA5681P

Fan Control
page 41

Clock Generator
IDT: 9LRS3199AKLFT
SILEGO: SLG8SP587
133/120/100/96/14.318MHZ to PCH
48MHZ to CardReader
page 12



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+GFX_core	Core voltage for CPU	ON	OFF	OFF
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+VGA_CORE	Core voltage for N11M VGA	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.5VS	1.5V power rail for DDRIII	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
PCH	
VGA	

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
Mini card	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA	UMA@
UMA only	UMA only@
DIS	DIS@
DIS Only	DIS only@
Switchable	SG@
	XDP@
	NonSG@
	MINI2@
	FP@
	eDriver@
	Dmic@
	Caps@
	X76@
	HDCP@
	AMIC@
S3 power	S3@
	non S3@

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port
		0	Ext4 HS USB
		1	sub Board
		2	
		3	Camera
		4	1st Min-Card
		5	2st Min-Card
		6	
		7	
		8	Ext4 HS USB
		9	Card Reader
		10	Blue Tooth
		11	Finger Print
		12	
		13	

BOM Config

UMA only
UMA@/UMA only@/FP@/Dmic@/XDP@/S3@

DIS ONLY

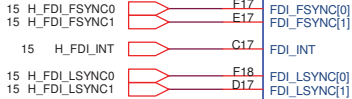
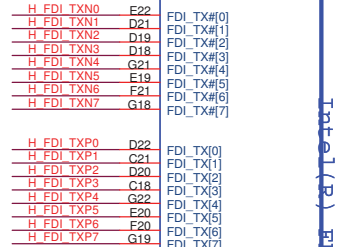
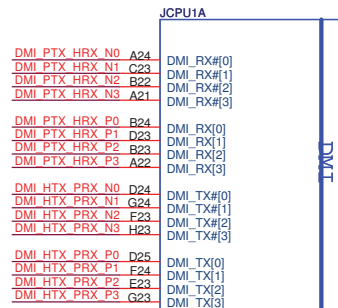
DIS@/DIS only@/FP@/Dmic@/XDP@/S3@

Switchable Graphics

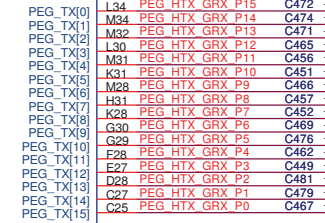
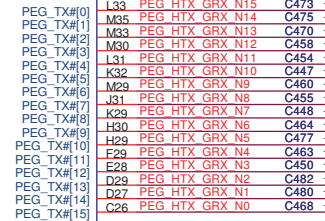
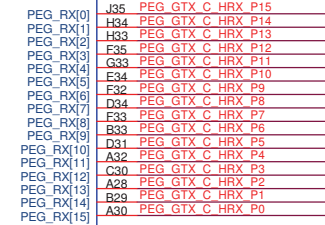
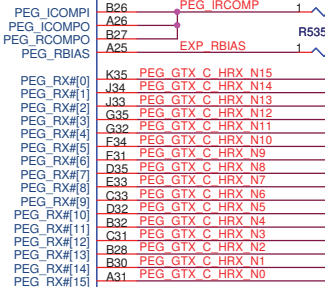
SG@/UMA@/DIS@/FP@/Dmic@/XDP@/S3@

Note:do cost BOM add X76@

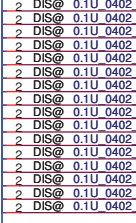
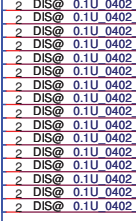
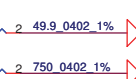
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								Date:		Friday, October 23, 2009	
								Sheet		3 of 60	



IC:AUB_CFD_rPGA,R1P0
CONN@



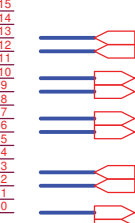
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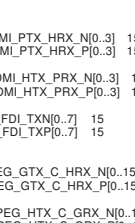
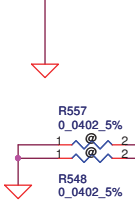
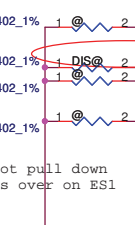
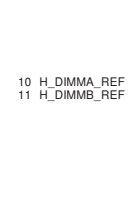
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CONN@



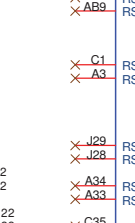
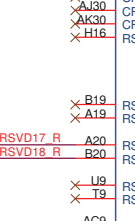
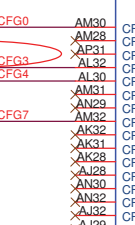
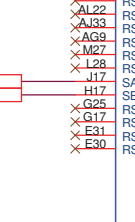
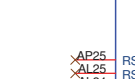
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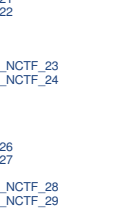
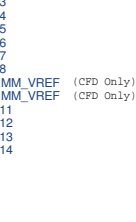
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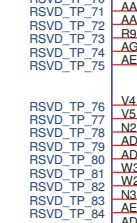
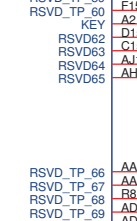
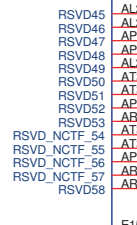
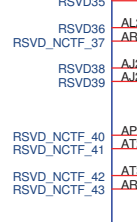
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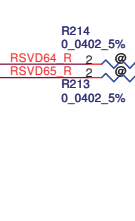
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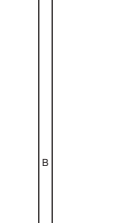
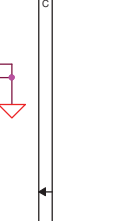
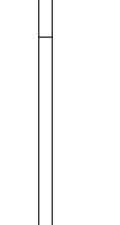
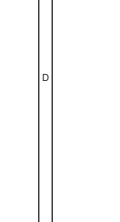
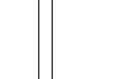
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CONN@



IC:AUB_CFD_rPGA,R1P0
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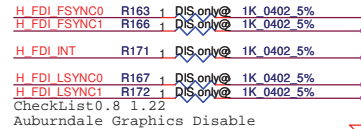
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CONN@



IC:AUB_CFD_rPGA,R1P0
CONN@

eDP Signals MAPPING

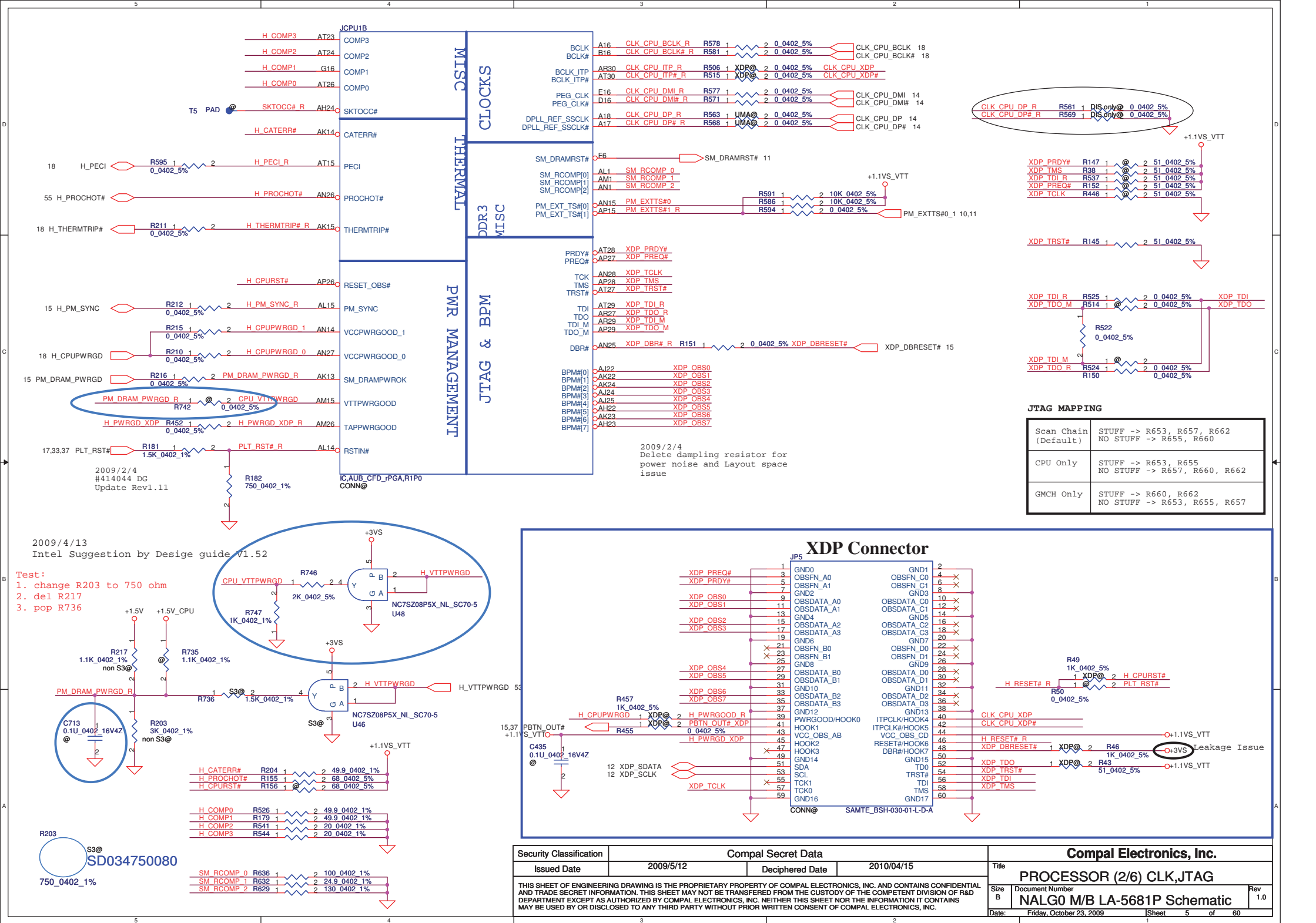
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eDP_TX1	PEG HTX_C_GRX_P14	PEG HTX_C_GRX_P1
eDP_TX#1	PEG HTX_C_GRX_N14	PEG HTX_C_GRX_N1
eDP_TX2	PEG HTX_C_GRX_P13	PEG HTX_C_GRX_P2
eDP_TX#2	PEG HTX_C_GRX_N13	PEG HTX_C_GRX_N2
eDP_TX3	PEG HTX_C_GRX_P12	PEG HTX_C_GRX_P3
eDP_TX#3	PEG HTX_C_GRX_N12	PEG HTX_C_GRX_N3
eDP_AUX	PEG GTX_C_HRX_P13	PEG GTX_C_HRX_P2
eDP_AUX#	PEG GTX_C_HRX_N13	PEG GTX_C_HRX_N2



CFG0 - PCI-Express Configuration Select
*1:Single PEG 0:Bifurcation enabled
CFG3 - PCI-Express Static Lane Reversal
*1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence
*1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port
*:Default

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10 DDR_A_D[0..63]
10 DDR_A_DM[0..7]
10 DDR_A_DQS[0..7]
10 DDR_A_MA[0..15]

JCPU1C

DDR A D0 A10
DDR A D1 C10
DDR A D2 C7
DDR A D3 A7
DDR A D4 B10
DDR A D5 D10
DDR A D6 E10
DDR A D7 A8
DDR A D8 D8
DDR A D9 F10
DDR A D10 E6
DDR A D11 E7
DDR A D12 E9
DDR A D13 B7
DDR A D14 E7
DDR A D15 C6
DDR A D16 H10
DDR A D17 G8
DDR A D18 K7
DDR A D19 J8
DDR A D20 G7
DDR A D21 G10
DDR A D22 J7
DDR A D23 J10
DDR A D24 L7
DDR A D25 M6
DDR A D26 M8
DDR A D27 L9
DDR A D28 L6
DDR A D29 K8
DDR A D30 N8
DDR A D31 P9
DDR A D32 AH5
DDR A D33 AF5
DDR A D34 AK6
DDR A D35 AK7
DDR A D36 AF6
DDR A D37 AG5
DDR A D38 AJ7
DDR A D39 AJ6
DDR A D40 AJ10
DDR A D41 AJ8
DDR A D42 AL10
DDR A D43 AK12
DDR A D44 AK8
DDR A D45 AL7
DDR A D46 AK11
DDR A D47 AL8
DDR A D48 AN8
DDR A D49 AM11
DDR A D50 AM11
DDR A D51 AL11
DDR A D52 AM9
DDR A D53 AN9
DDR A D54 AT11
DDR A D55 AP12
DDR A D56 AM12
DDR A D57 AN12
DDR A D58 AM13
DDR A D59 AT14
DDR A D60 AT12
DDR A D61 AL13
DDR A D62 AR14
DDR A D63 AP14

10 DDR_A_BS0
10 DDR_A_BS1
10 DDR_A_BS2

10 DDR_A_CAS#
10 DDR_A_RAS#
10 DDR_A_WE#

DDR SYSTEM MEMORY - A

SA_CK[0] AA6
SA_CK#0 AA7
SA_CKE[0] P7
SA_CK[1] Y6
SA_CK#1 Y6
SA_CKE[1] P6
SA_CS#0 AE2
SA_CS#1 AE8
SA_ODT[0] AD8
SA_ODT[1] AF9
SA_DM[0] B9
SA_DM[1] D7
SA_DM[2] H7
SA_DM[3] M7
SA_DM[4] AG6
SA_DM[5] AM7
SA_DM[6] AN10
SA_DM[7] AN13
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SA_DQS#1 E8
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SA_DQS#6 AT13
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SA_MA[7] T1
SA_MA[8] Y9
SA_MA[9] U6
SA_MA[10] AD4
SA_MA[11] U3
SA_MA[12] AG8
SA_MA[13] T3
SA_MA[14] V9
SA_MA[15]

IC:AUB_CFD_rPGA,R1P0
CONN@

11 DDR_B_D[0..63]
11 DDR_B_DM[0..7]
11 DDR_B_DQS[0..7]
11 DDR_B_MA[0..15]

JCPU1D

DDR B D0 B5
DDR B D1 B5
DDR B D2 C3
DDR B D3 B3
DDR B D4 E4
DDR B D5 A6
DDR B D6 C4
DDR B D7 A4
DDR B D8 D1
DDR B D9 D2
DDR B D10 F2
DDR B D11 F1
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DDR B D58 AP8
DDR B D59 AT9
DDR B D60 AT7
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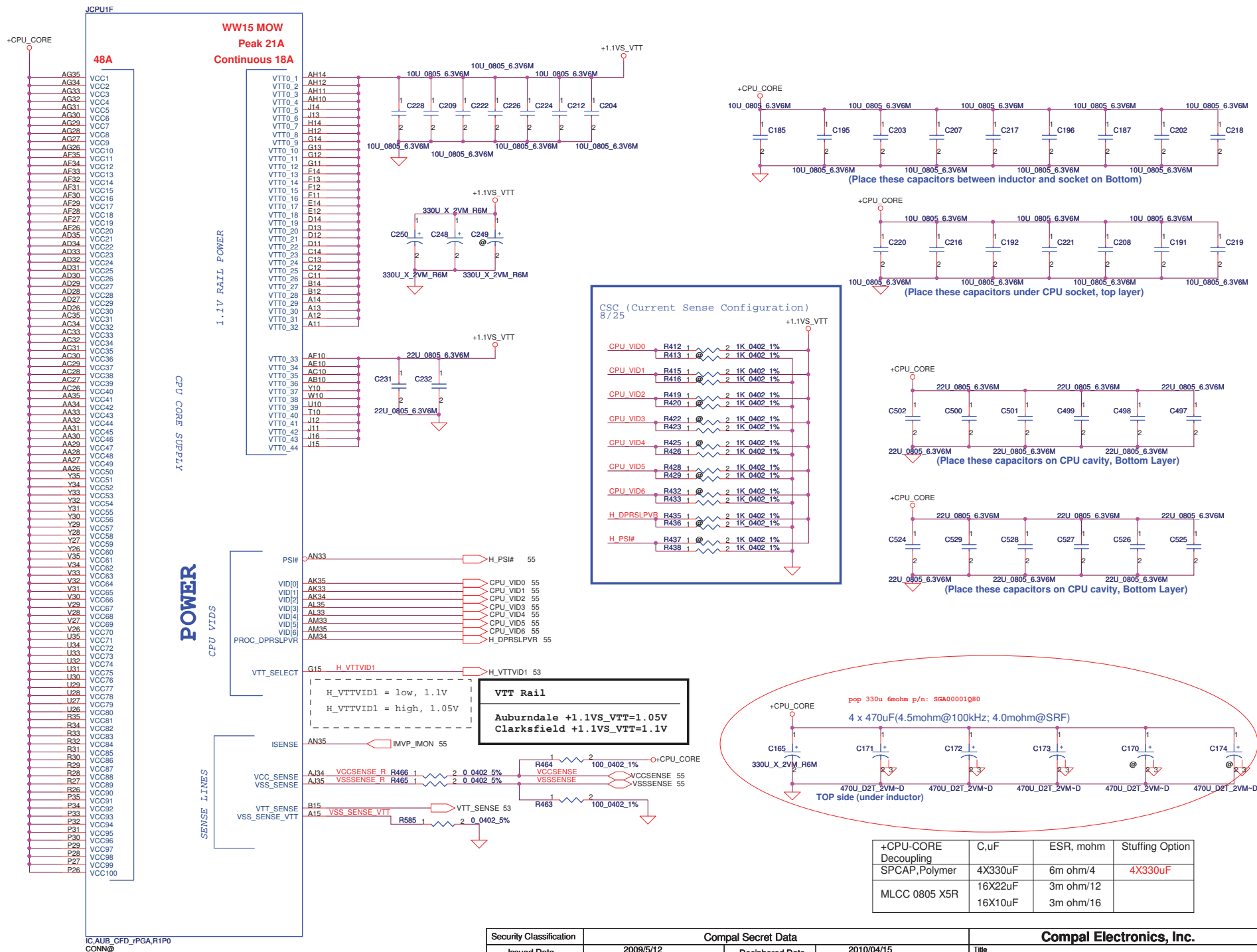
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11 DDR_B_RAS#
11 DDR_B_WE#

DDR SYSTEM MEMORY - B

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SB_CK#0 W9
SB_CKE[0] M3
SB_CK[1] V7
SB_CK#1 V6
SB_CKE[1] M2
SB_CS#0 AB8
SB_CS#1 AD6
SB_ODT[0] AC7
SB_ODT[1] AD1
SB_DM[0] D4
SB_DM[1] E1
SB_DM[2] H3
SB_DM[3] K1
SB_DM[4] AH1
SB_DM[5] AL2
SB_DM[6] AR4
SB_DM[7] AT8
SB_DQS#0 D5
SB_DQS#1 E4
SB_DQS#2 D4
SB_DQS#3 L4
SB_DQS#4 AH2
SB_DQS#5 AL4
SB_DQS#6 AR5
SB_DQS#7 AR8
SB_DQS[0] C5
SB_DQS[1] E3
SB_DQS[2] H4
SB_DQS[3] M5
SB_DQS[4] AG2
SB_DQS[5] AP5
SB_DQS[6] AR7
SB_DQS[7]
SB_MA[0] U5
SB_MA[1] V2
SB_MA[2] T5
SB_MA[3] V3
SB_MA[4] B1
SB_MA[5] T8
SB_MA[6] B2
SB_MA[7] B6
SB_MA[8] B4
SB_MA[9] R5
SB_MA[10] AR5
SB_MA[11] P3
SB_MA[12] R3
SB_MA[13] AF7
SB_MA[14] P5
SB_MA[15] N1

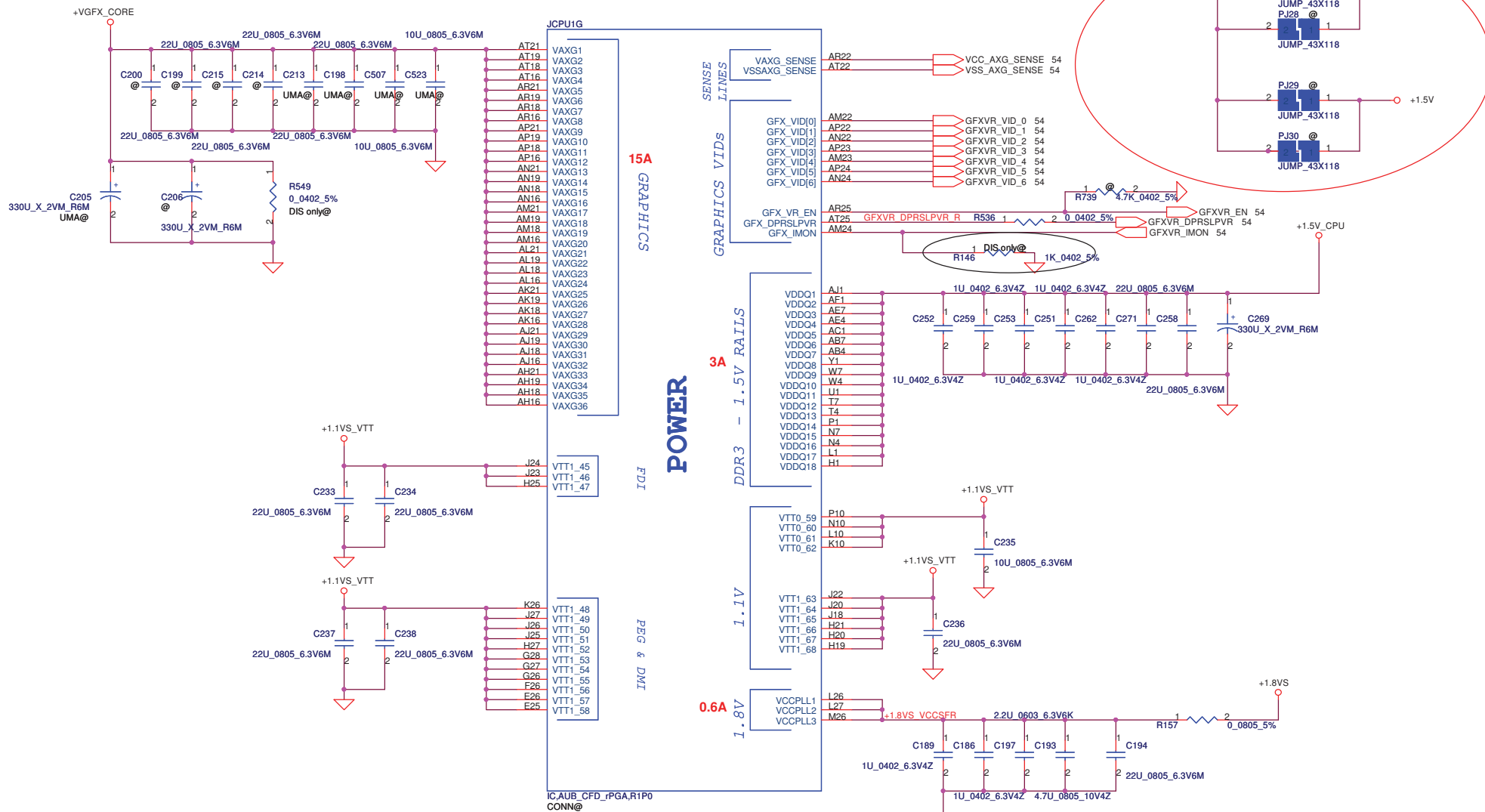
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CONN@

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Issued Date		2009/5/12		Deciphered Date		2010/04/15		Title		
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								Size	Document Number	Rev
								B	NALG0 M/B LA-5681P Schematic	1.0
								Date:	Friday, October 23, 2009	Sheet

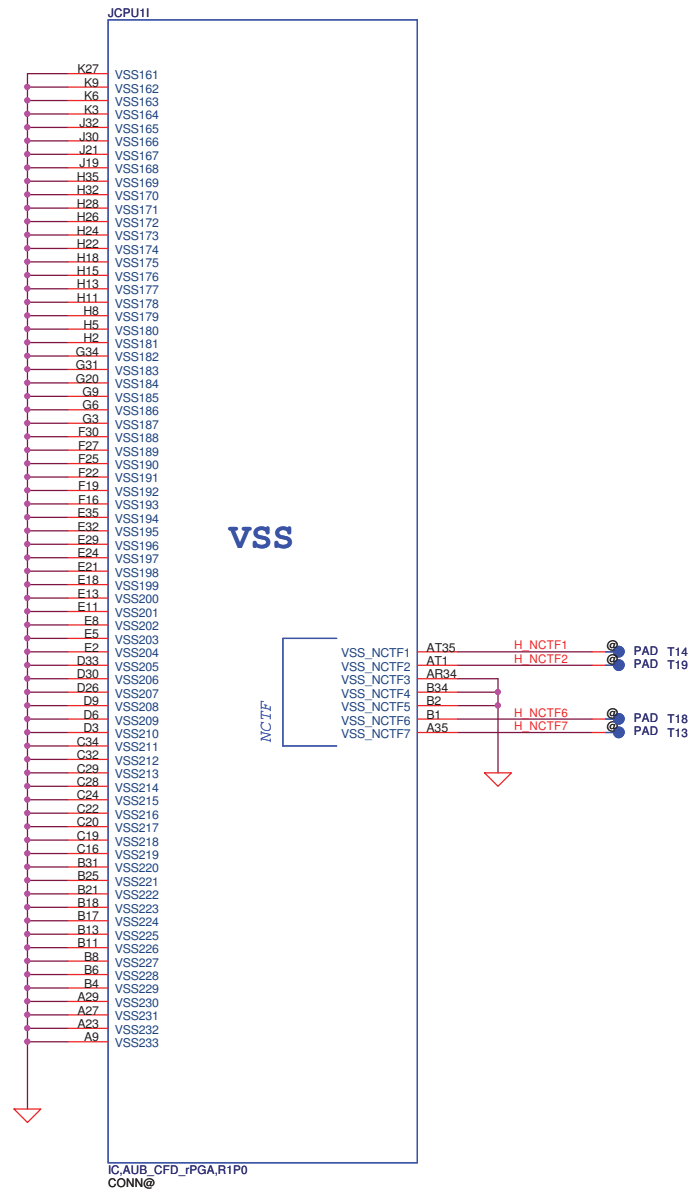
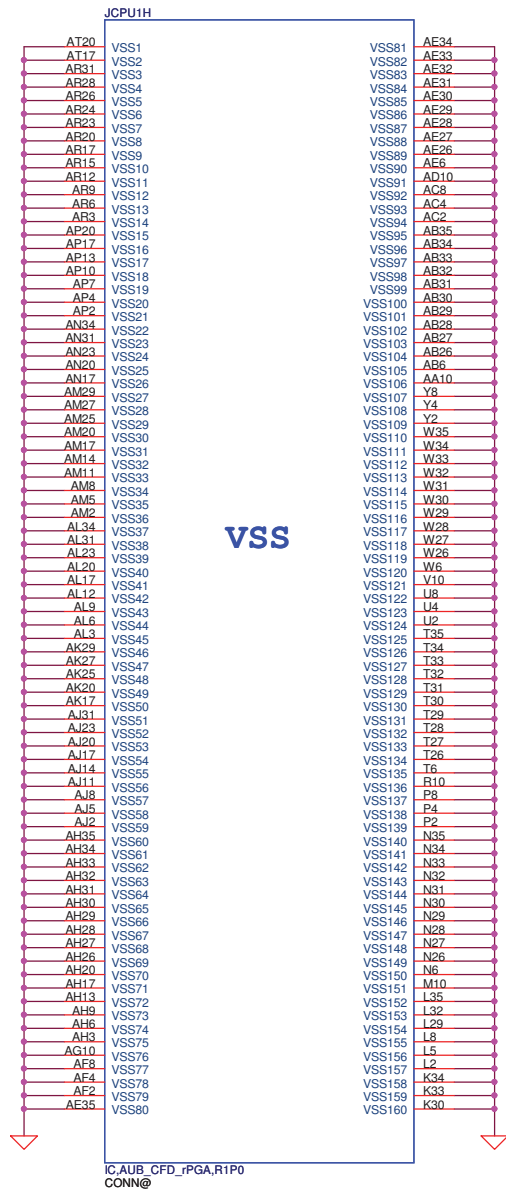


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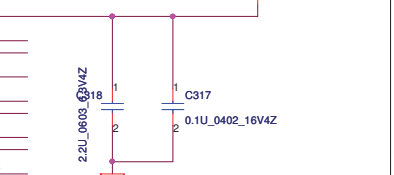
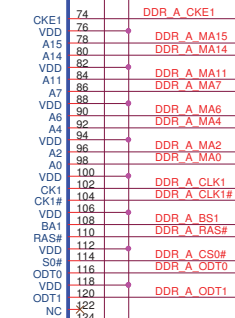
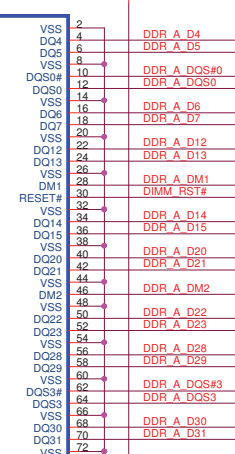
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Issued Date	2009/5/12	Deciphered Date	2010/04/15	Title
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Customer				Document Number
Date				Revision
Friday, October 23, 2009				1
Sheet				7 of 60



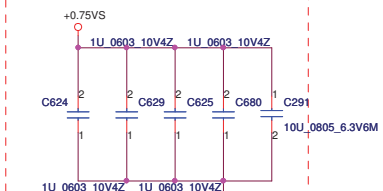
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Issued Date	2009/5/12	Deciphered Date	2010/04/15	Title	
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Size	Custom	Document Number	NALG0 M/B LA-5681P Schematic		Rev
Date	Friday, October 23, 2009	Sheet	8	of	60



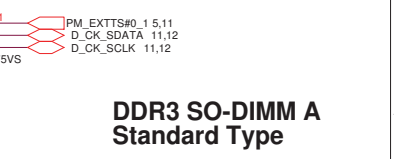
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Issued Date		2009/5/12		Deciphered Date		2010/04/15		
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				PROCESSOR (6/6) VSS				
				Size	Document Number			Rev
				Customer	NALG0 M/B LA-5681P Schematic			1.0
				Date:	Friday, October 23, 2009		Sheet 9 of 60	



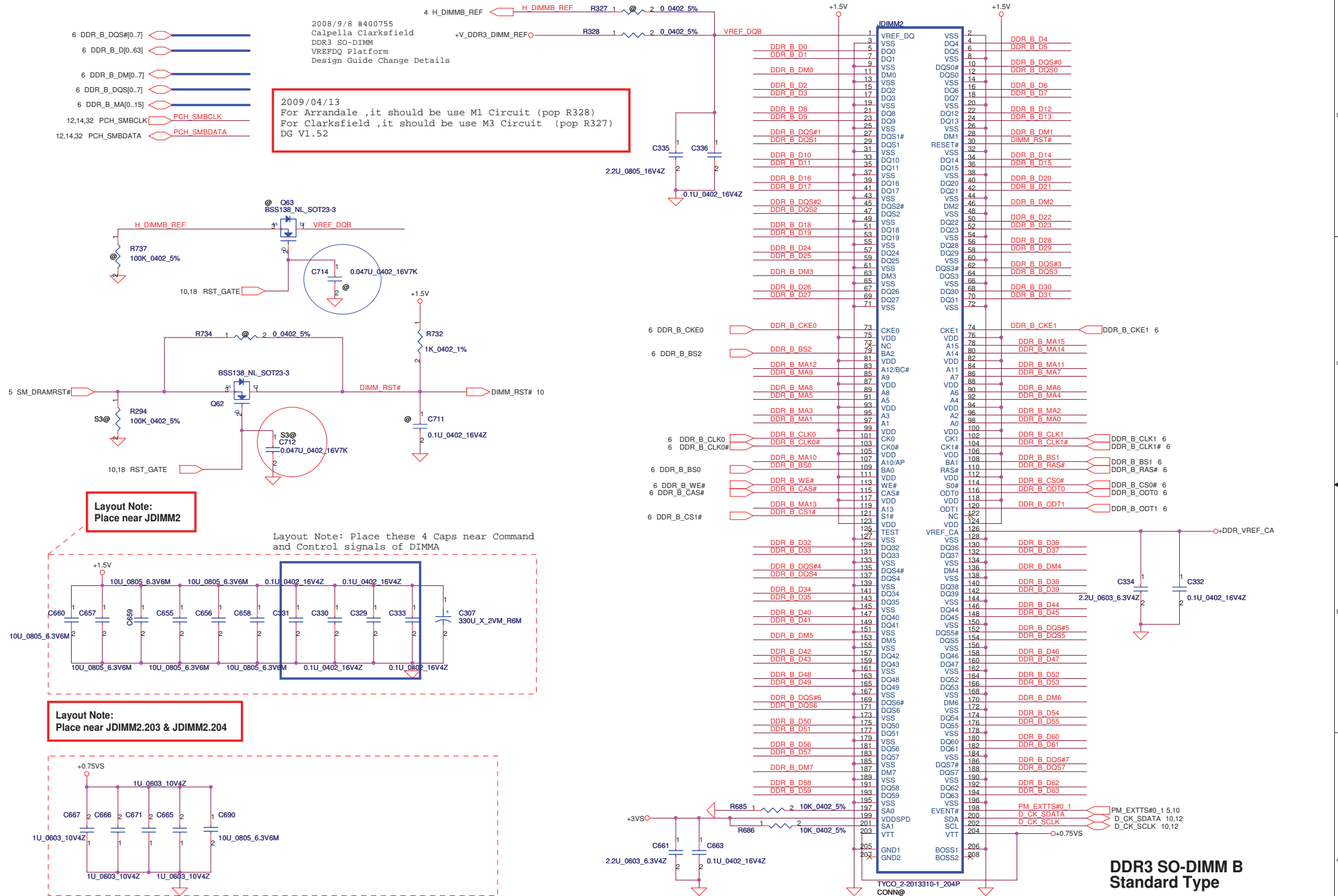
Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



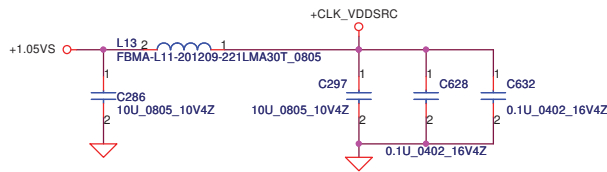
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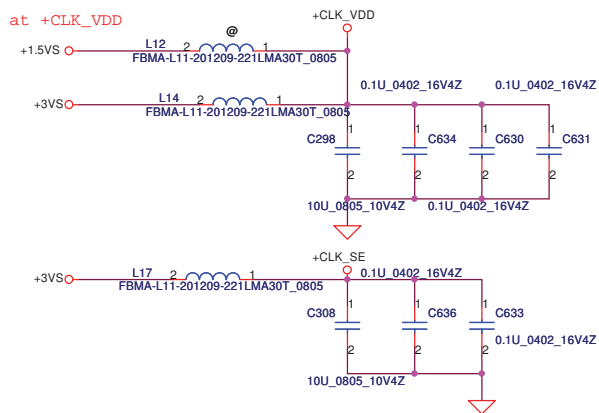
Security Classification	Compal Secret Data			Compal Electronics, Inc. DDRIII-SODIMM SLOT1		
Issued Date	2009/5/12	Deciphered Date	2010/04/15	Rev 1.0 NALGO M/B LA-5681P Schematic		
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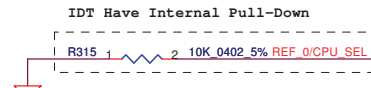
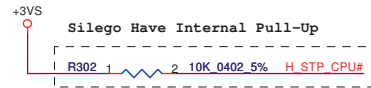
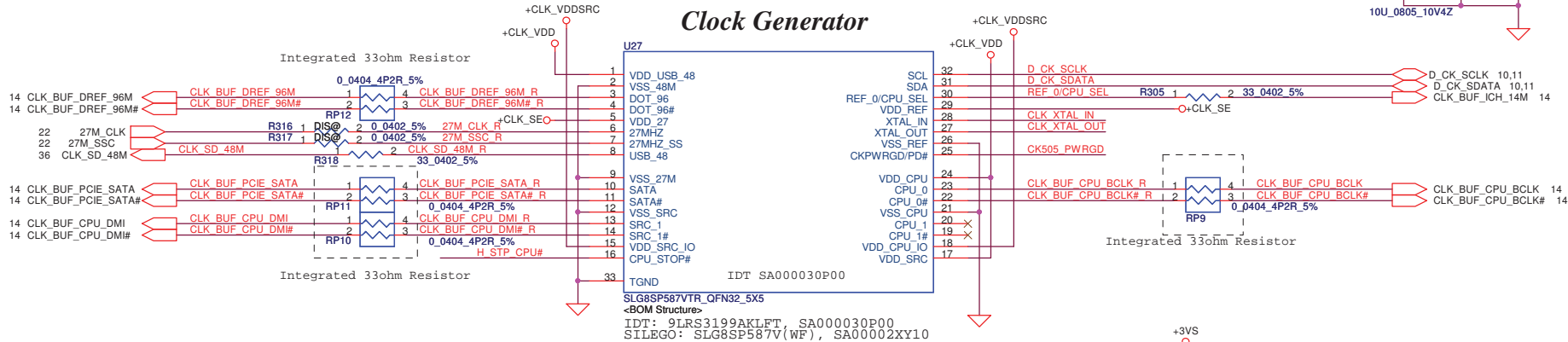
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Issued Date		2009/5/12		Deciphered Date		2010/04/15		DDRIII-SODIMM SLOT2			
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						Document Number		Rev			
						Date		Sheet			
						Friday, October 23, 2009		11 of 60			



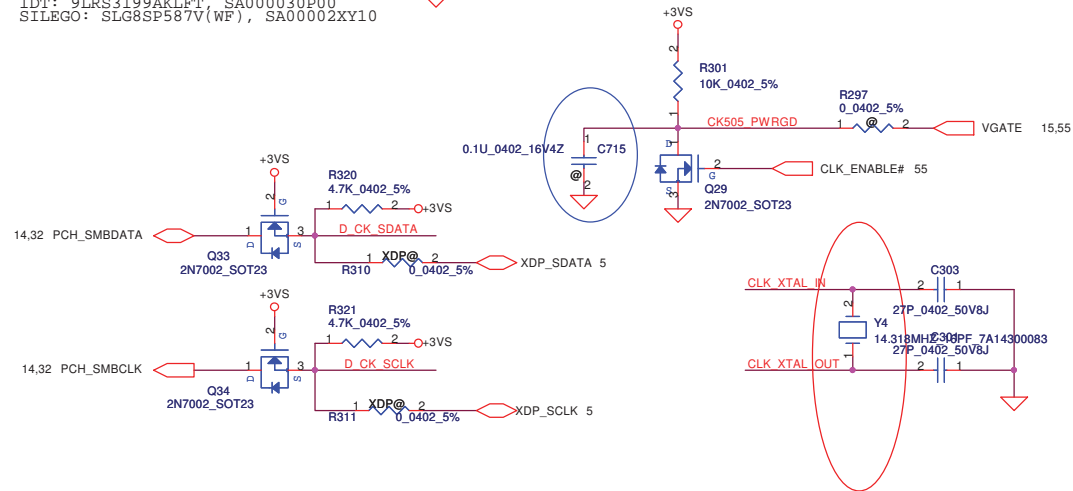
power save CLK gen use +1.5VS at +CLK_VDD



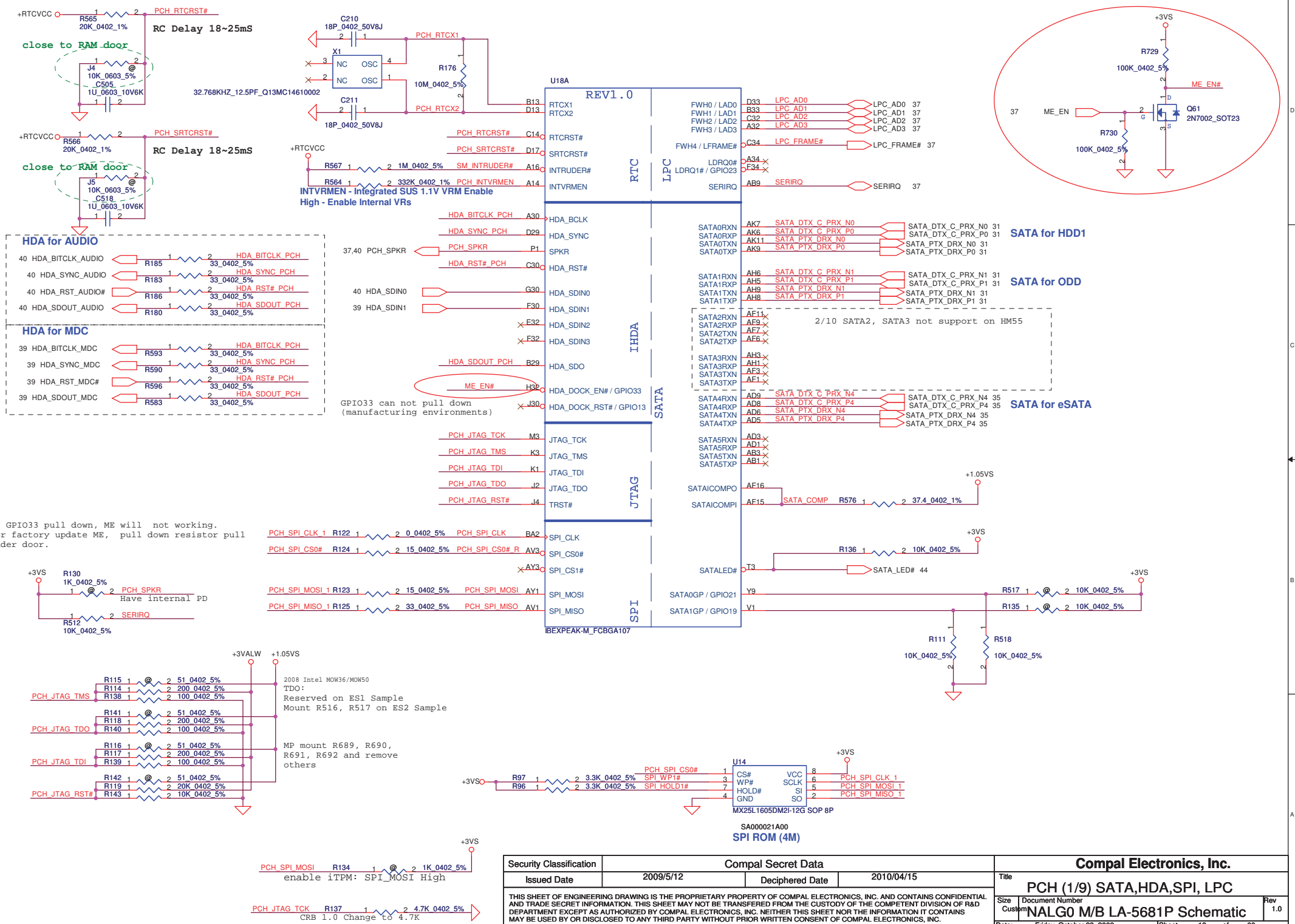
Clock Generator



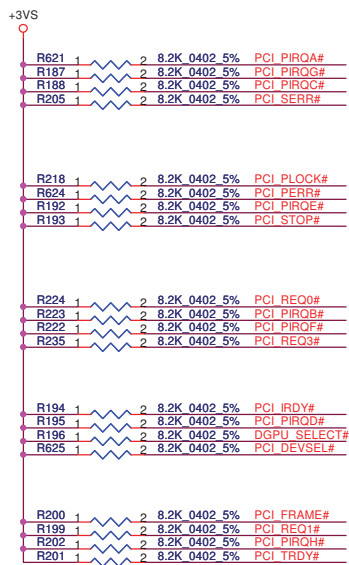
PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz



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Size	Document Number	Customer	NALG0 M/B LA-5681P Schematic	Rev	1.0
Date:	Friday, October 23, 2009	Sheet	12	of	60



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Issued Date	2009/5/12	Deciphered Date	2010/04/15	Title PCH (1/9) SATA,HDA,SPI, LPC			
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				Custom	NALGO M/B LA-5681P Schematic	1.0	
Date:				Friday, October 23, 2009	Sheet	13 of 60	



28,29 DGPU_SELECT#

28 DGPU_PWMSEL#

5,33,37 PLT_RST#

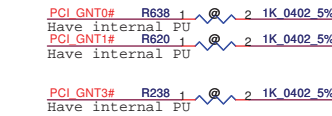
37 CLK_PCI_LPC

14 CLK_PCI_FB

2008/1/6 2009MOW01 change to 22 ohm

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default



PCI

USB

IBEXPEAK-M_FCBGA107



USBRBIAS#

USBRBIAS



OC0# / GPIO59

OC1# / GPIO40

OC2# / GPIO41

OC3# / GPIO42

OC4# / GPIO43

OC5# / GPIO48

OC6# / GPIO10

OC7# / GPIO14

OC8# / GPIO59

OC9# / GPIO40

OC10# / GPIO41

OC11# / GPIO42

OC12# / GPIO43

OC13# / GPIO48

OC14# / GPIO10

OC15# / GPIO14

OC16# / GPIO59

OC17# / GPIO40

OC18# / GPIO41

OC19# / GPIO42

OC20# / GPIO43

OC21# / GPIO48

OC22# / GPIO10

OC23# / GPIO14

OC24# / GPIO59

OC25# / GPIO40

OC26# / GPIO41

OC27# / GPIO42

OC28# / GPIO43

OC29# / GPIO48

OC30# / GPIO10

OC31# / GPIO14

OC32# / GPIO59

OC33# / GPIO40

OC34# / GPIO41

OC35# / GPIO42

OC36# / GPIO43

OC37# / GPIO48

OC38# / GPIO10

OC39# / GPIO14

OC40# / GPIO59

OC41# / GPIO40

OC42# / GPIO41

OC43# / GPIO42

OC44# / GPIO43

OC45# / GPIO48

OC46# / GPIO10

OC47# / GPIO14

OC48# / GPIO59

OC49# / GPIO40

OC50# / GPIO41

OC51# / GPIO42

OC52# / GPIO43

OC53# / GPIO48

OC54# / GPIO10

OC55# / GPIO14

OC56# / GPIO59

OC57# / GPIO40

OC58# / GPIO41

OC59# / GPIO42

OC60# / GPIO43

OC61# / GPIO48

OC62# / GPIO10

OC63# / GPIO14

OC64# / GPIO59

OC65# / GPIO40

OC66# / GPIO41

OC67# / GPIO42

OC68# / GPIO43

OC69# / GPIO48

OC70# / GPIO10

OC71# / GPIO14

OC72# / GPIO59

OC73# / GPIO40

OC74# / GPIO41

OC75# / GPIO42

OC76# / GPIO43

OC77# / GPIO48

OC78# / GPIO10

OC79# / GPIO14

OC80# / GPIO59

OC81# / GPIO40

OC82# / GPIO41

OC83# / GPIO42

OC84# / GPIO43

OC85# / GPIO48

OC86# / GPIO10

OC87# / GPIO14

OC88# / GPIO59

OC89# / GPIO40

OC90# / GPIO41

OC91# / GPIO42

OC92# / GPIO43

OC93# / GPIO48

OC94# / GPIO10

OC95# / GPIO14

OC96# / GPIO59

OC97# / GPIO40

OC98# / GPIO41

OC99# / GPIO42

OC100# / GPIO43

OC101# / GPIO48

OC102# / GPIO10

OC103# / GPIO14

OC104# / GPIO59

OC105# / GPIO40

OC106# / GPIO41

OC107# / GPIO42

OC108# / GPIO43

OC109# / GPIO48

OC110# / GPIO10

OC111# / GPIO14

OC112# / GPIO59

OC113# / GPIO40

OC114# / GPIO41

OC115# / GPIO42

OC116# / GPIO43

OC117# / GPIO48

OC118# / GPIO10

OC119# / GPIO14

OC120# / GPIO59

OC121# / GPIO40

OC122# / GPIO41

OC123# / GPIO42

OC124# / GPIO43

OC125# / GPIO48

OC126# / GPIO10

OC127# / GPIO14

OC128# / GPIO59

OC129# / GPIO40

OC130# / GPIO41

OC131# / GPIO42

OC132# / GPIO43

OC133# / GPIO48

OC134# / GPIO10

OC135# / GPIO14

OC136# / GPIO59

OC137# / GPIO40

OC138# / GPIO41

OC139# / GPIO42

OC140# / GPIO43

OC141# / GPIO48

OC142# / GPIO10

OC143# / GPIO14

OC144# / GPIO59

OC145# / GPIO40

OC146# / GPIO41

OC147# / GPIO42

OC148# / GPIO43

OC149# / GPIO48

OC150# / GPIO10

OC151# / GPIO14

OC152# / GPIO59

OC153# / GPIO40

OC154# / GPIO41

OC155# / GPIO42

OC156# / GPIO43

OC157# / GPIO48

OC158# / GPIO10

OC159# / GPIO14

OC160# / GPIO59

OC161# / GPIO40

OC162# / GPIO41

OC163# / GPIO42

OC164# / GPIO43

OC165# / GPIO48

OC166# / GPIO10

OC167# / GPIO14

OC168# / GPIO59

OC169# / GPIO40

OC170# / GPIO41

OC171# / GPIO42

OC172# / GPIO43

OC173# / GPIO48

OC174# / GPIO10

OC175# / GPIO14

OC176# / GPIO59

OC177# / GPIO40

OC178# / GPIO41

OC179# / GPIO42

OC180# / GPIO43

OC181# / GPIO48

OC182# / GPIO10

OC183# / GPIO14

OC184# / GPIO59

OC185# / GPIO40

OC186# / GPIO41

OC187# / GPIO42

OC188# / GPIO43

OC189# / GPIO48

OC190# / GPIO10

OC191# / GPIO14

OC192# / GPIO59

OC193# / GPIO40

OC194# / GPIO41

OC195# / GPIO42

OC196# / GPIO43

OC197# / GPIO48

OC198# / GPIO10

OC199# / GPIO14

OC200# / GPIO59

OC201# / GPIO40

OC202# / GPIO41

OC203# / GPIO42

OC204# / GPIO43

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OC206# / GPIO10

OC207# / GPIO14

OC208# / GPIO59

OC209# / GPIO40

OC210# / GPIO41

OC211# / GPIO42

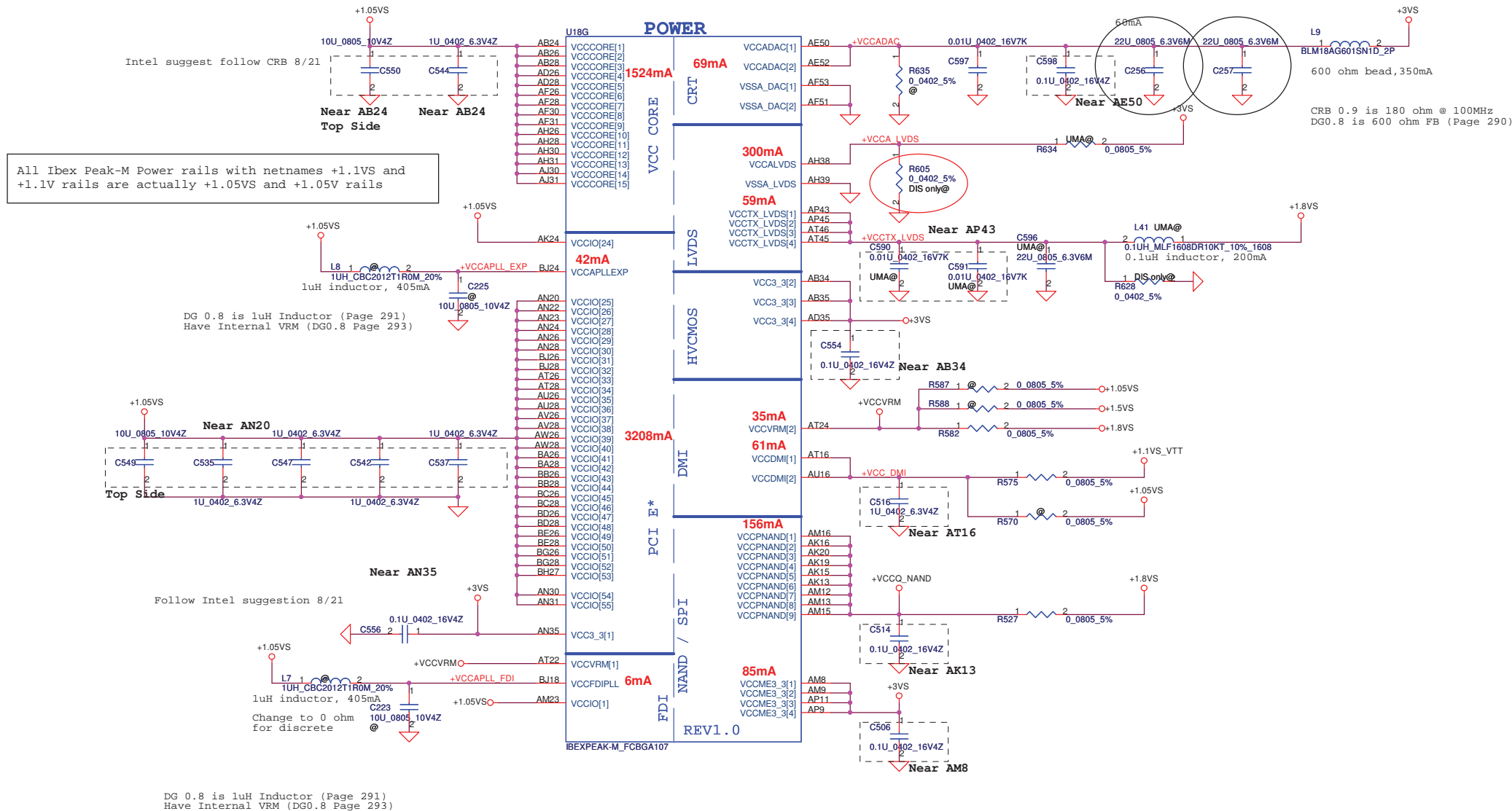
OC212# / GPIO43

OC213# / GPIO48

OC214# / GPIO10

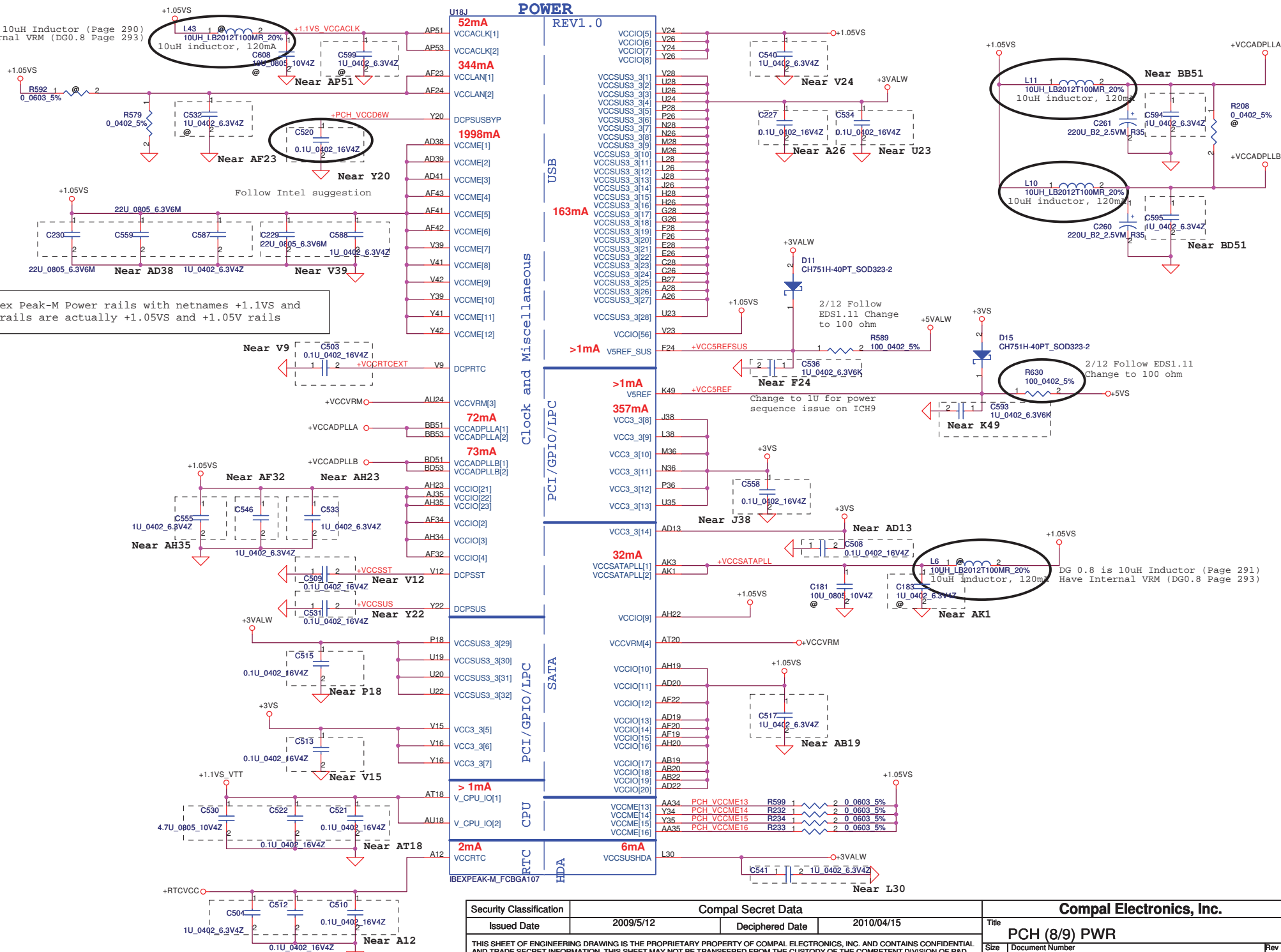
OC215# / GPIO14

OC216# / GPIO59



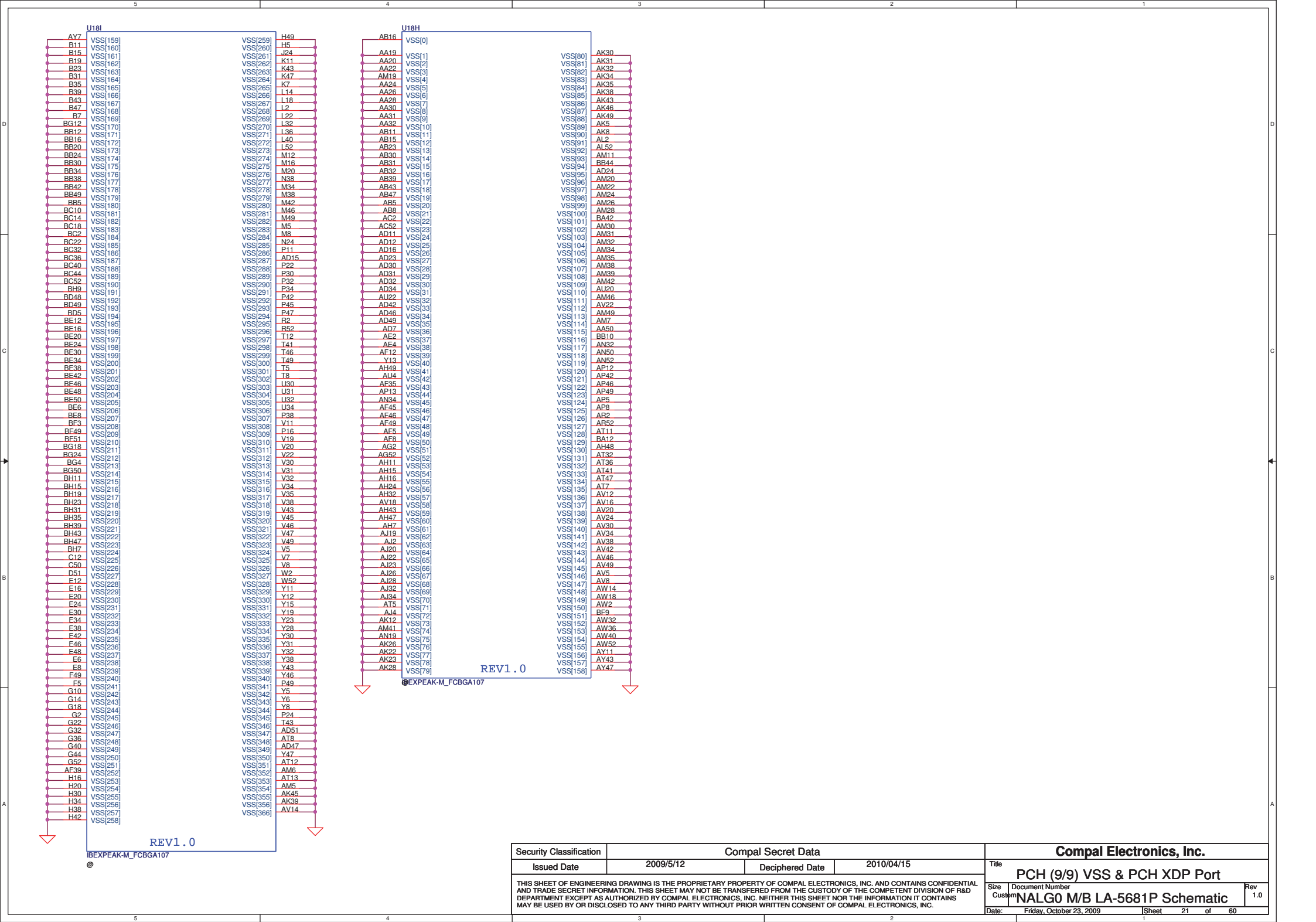
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				Document Number	NALG0 M/B LA-5681P Schematic
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				Rev	1.0

DG 0.8 is 10uH Inductor (Page 290)
Have Internal VRM (DG0.8 Page 293)



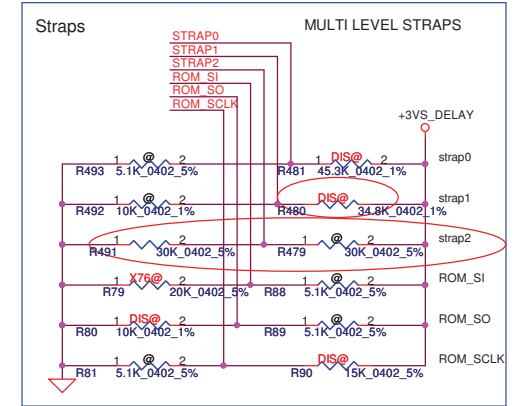
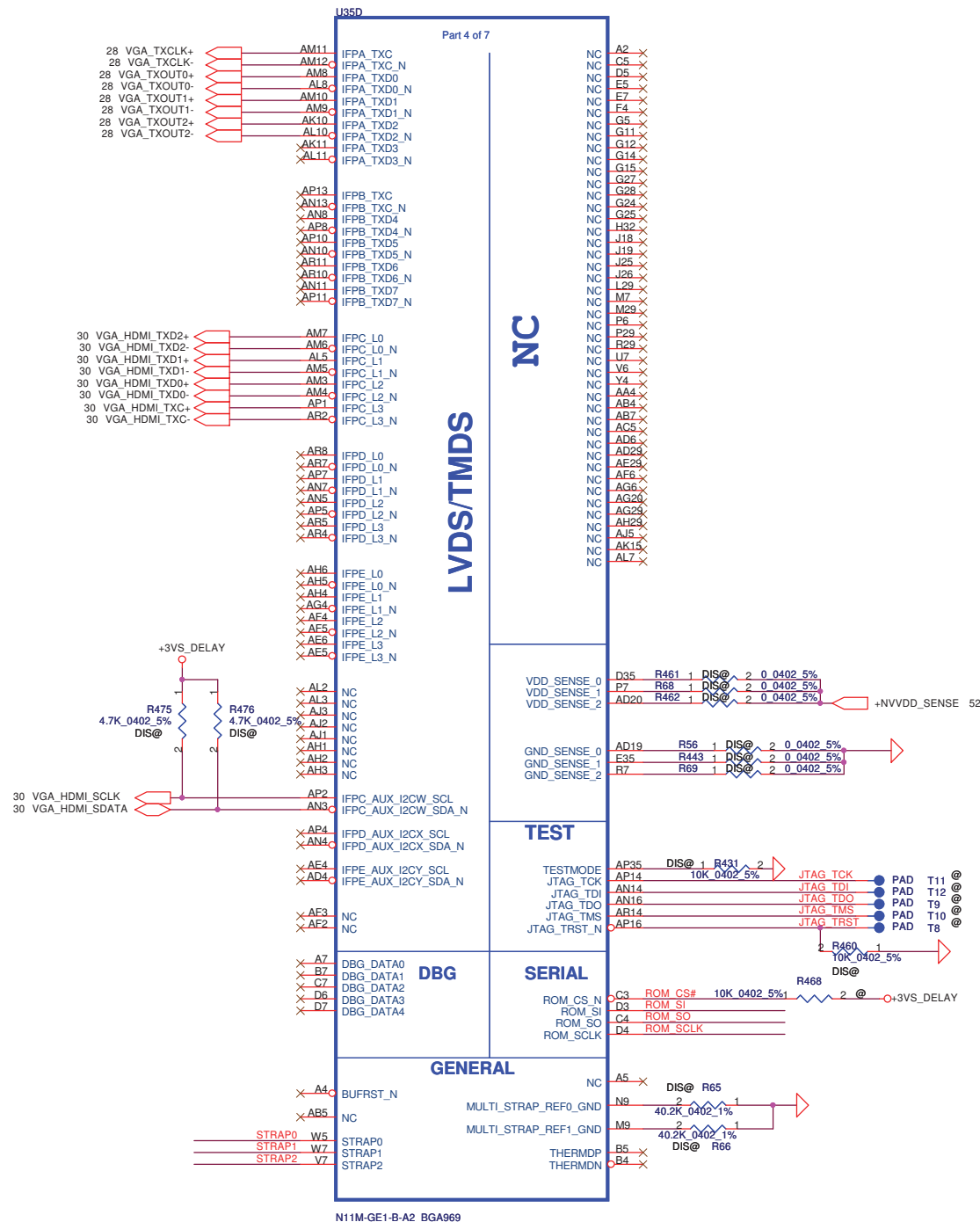
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		Size	Document Number						Rev
		Customer	NALG0 M/B LA-5681P Schematic						1.0
		Date:	Friday, October 23, 2009		Sheet	21	of	60	





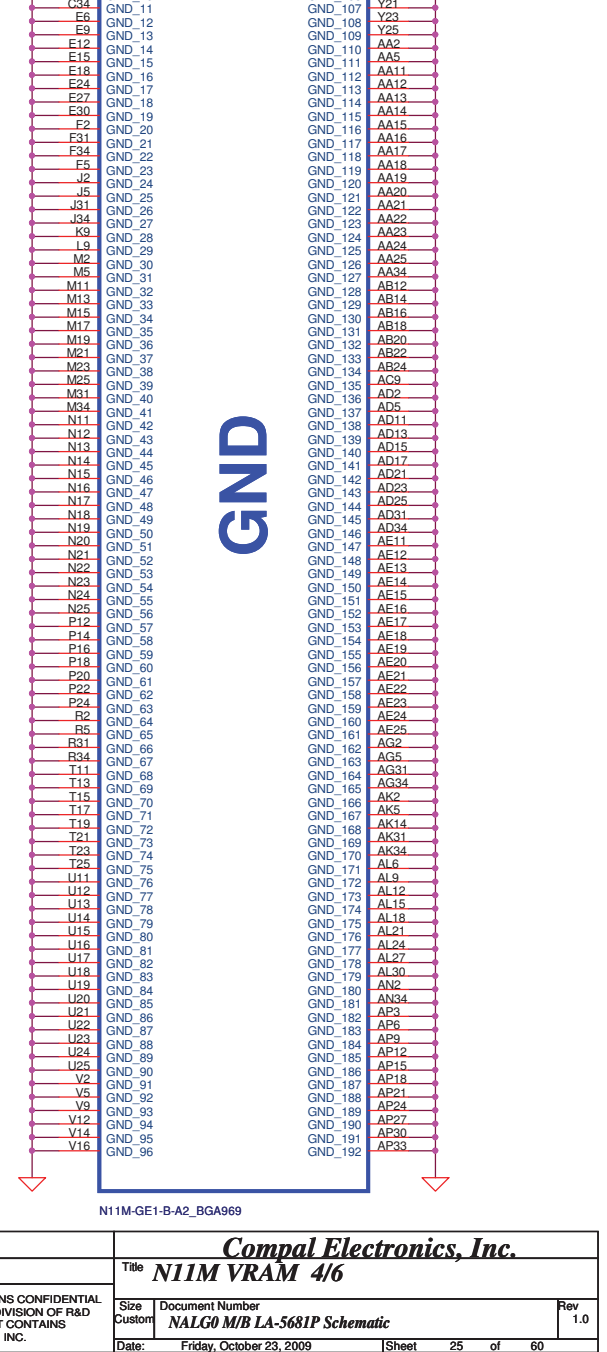
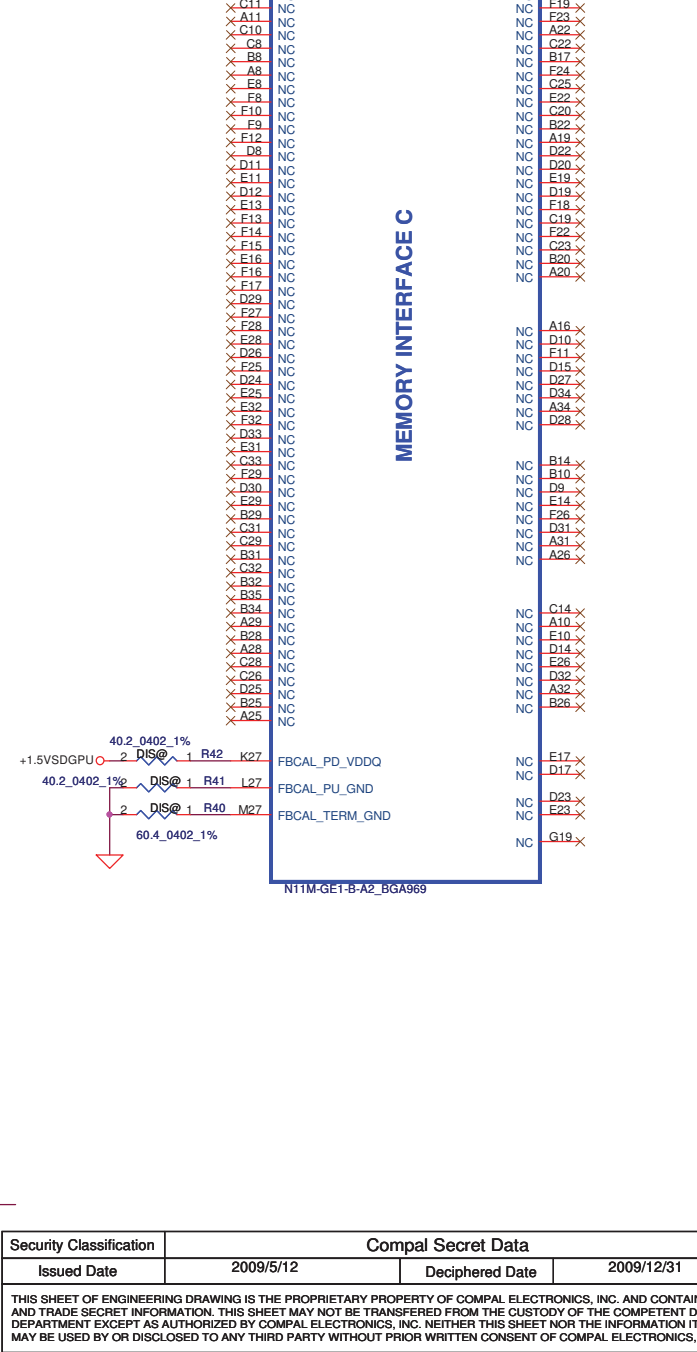
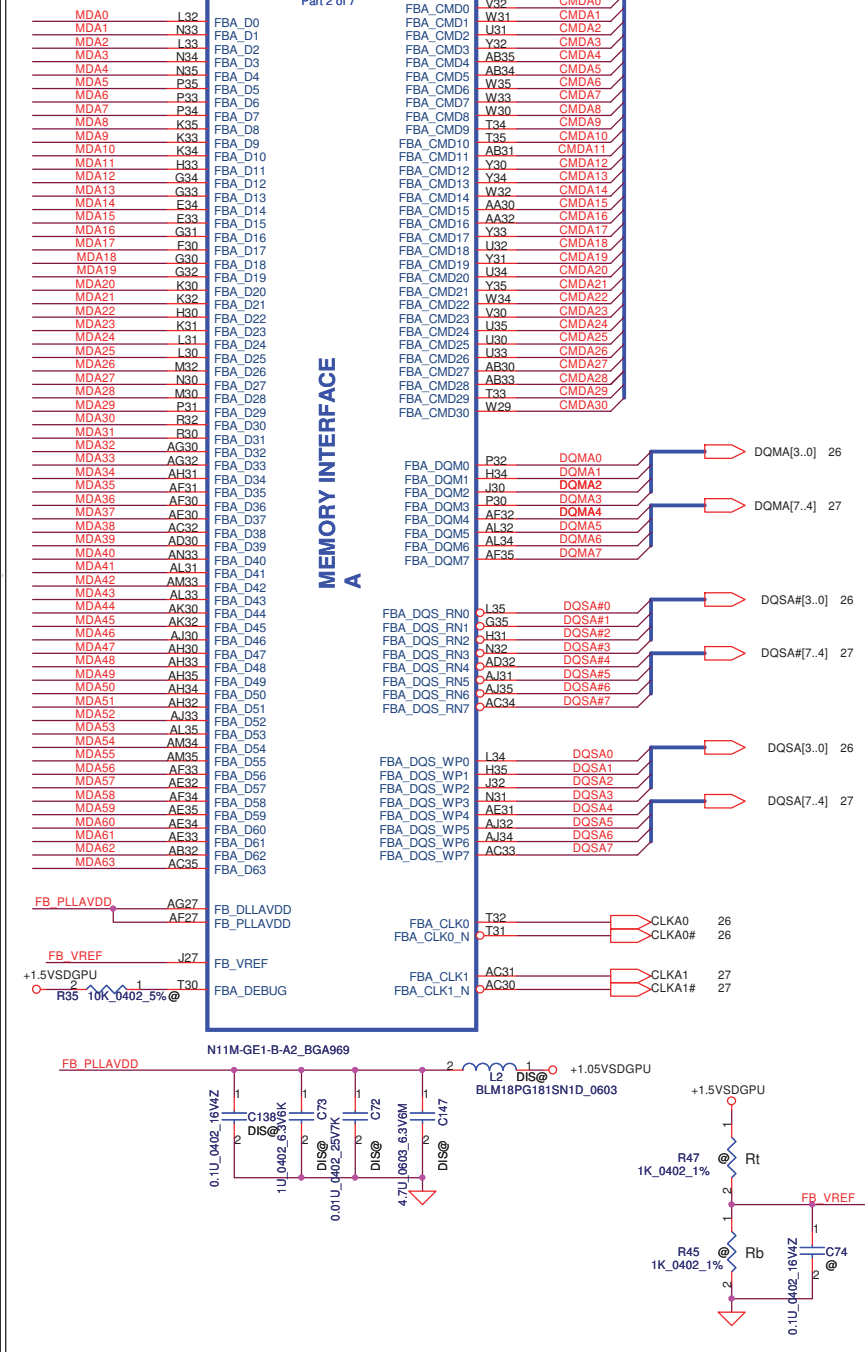
ES: pop R479 30K ohm
GS: pop R491 30K ohm
MP ID check R491 and R479

	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung SA000035700	H 45K	H 35K	L 30K	L 20K	L 10K	H 15K
64MX16 Hynix SA000032400	H 45K	H 35K	L 30K	L 15K	L 10K	H 15K

N11M-GE1-B-A2_BGA969

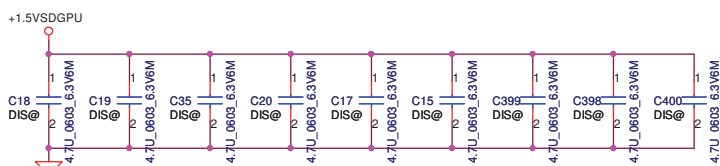
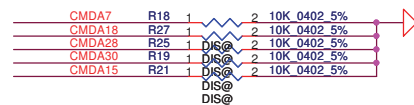
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Issued Date		2009/5/12		Deciphered Date		2010/04/15		Title		
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								Size	Document Number	Rev
								Custom	NALG0 M/B LA-5681P Schematic	
								Date:	Friday, October 23, 2009	Sheet 23 of 60

U35B



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Issued Date	2009/5/12	Deciphered Date	2009/12/31	Size Custom	Document Number <i>NALGO M/B LA-5681P Schematic</i>
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				Date: Friday, October 23, 2009 Sheet 25 of 60	

64Mx16 gDDR3 *4==>512MB



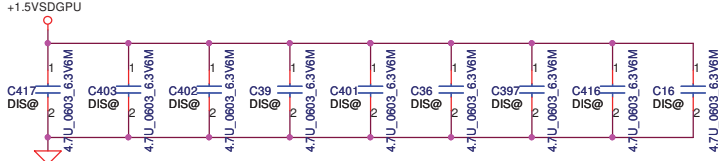
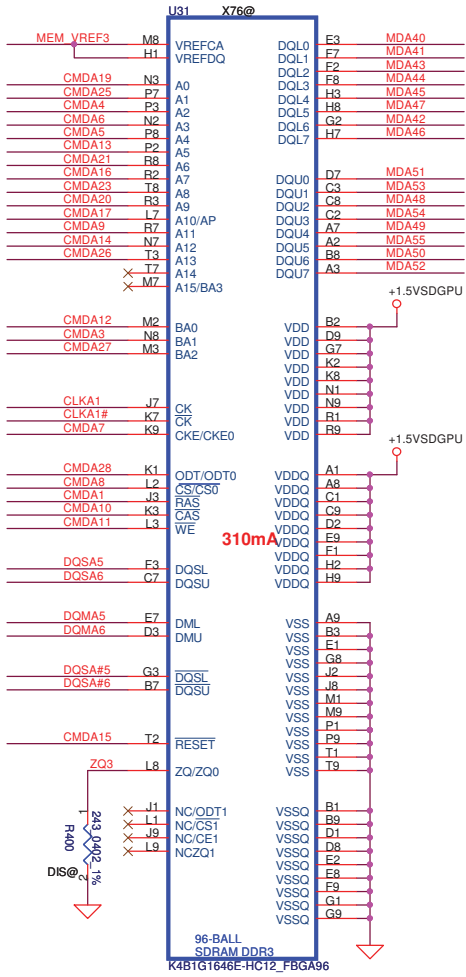
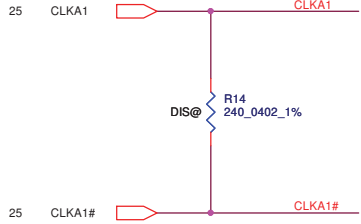
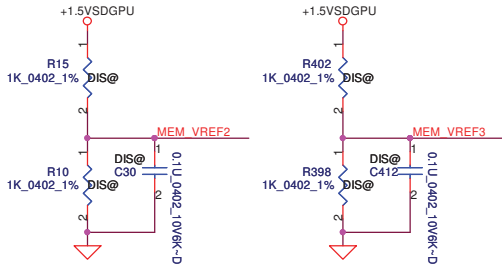
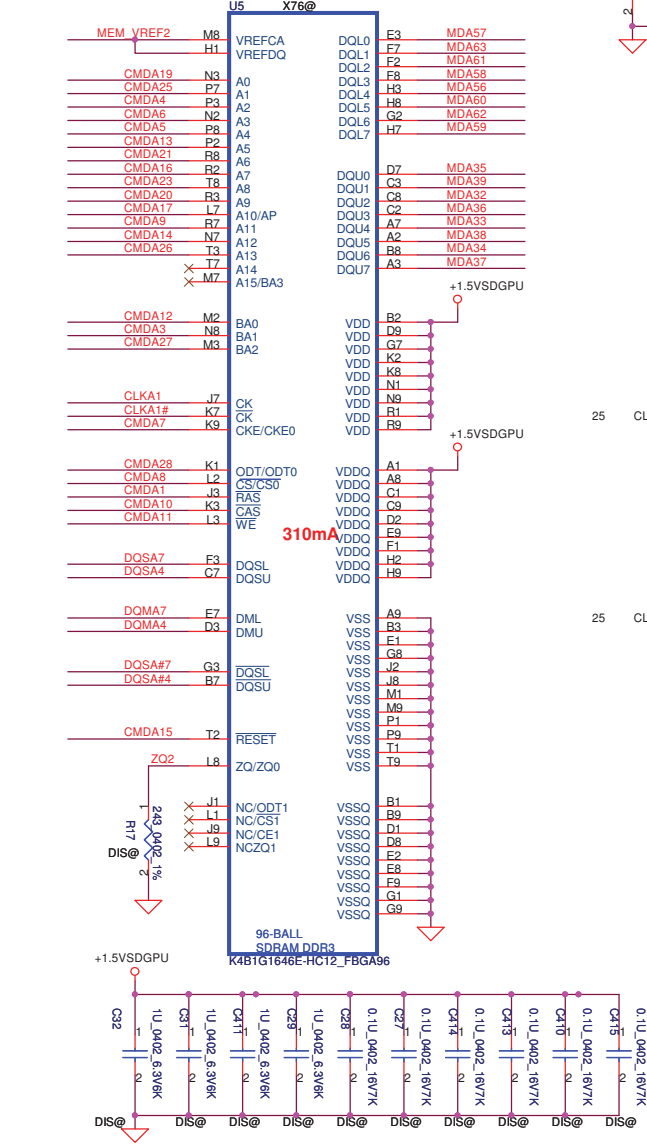
LOW	HIGH
-----	------

VRAM DDR3 chips (256MB & 512MB)

32Mx16 DDR3 *4==>256MB

64Mx16 DDR3 *4==>512MB

- 25,26 DQMA[7..0] DQMA[7..0]
- 25,26 CMDA[30..0] CMDA[30..0]
- 25,26 DQSA# [7..0] DQSA# [7..0]
- 25,26 DQSA [7..0] DQSA [7..0]
- 25,26 MDA[63..0] MDA[63..0]

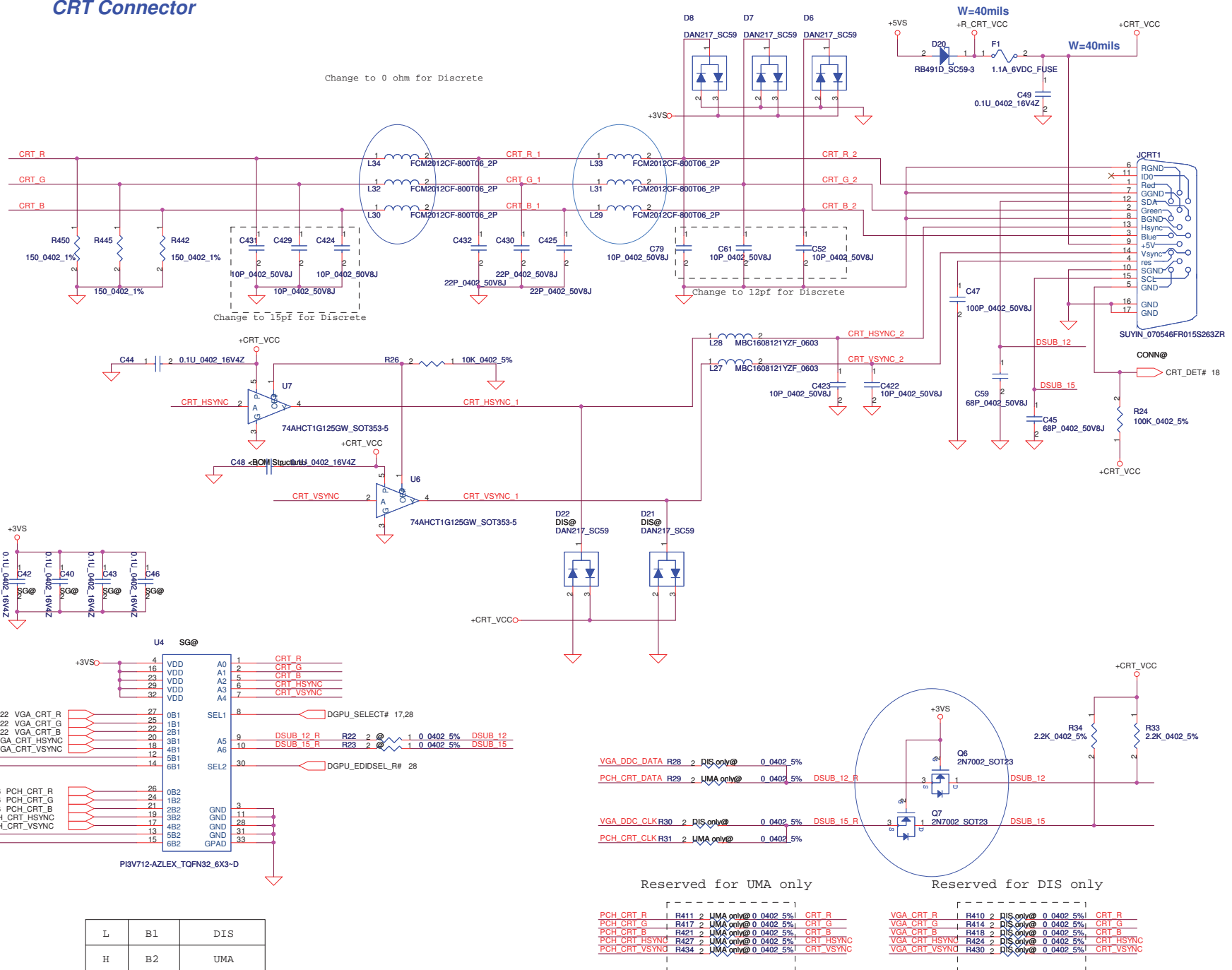


Address	0..31	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7		CKE
CMD8		CS#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS#	
CMD30	ODT	

LOW HIGH

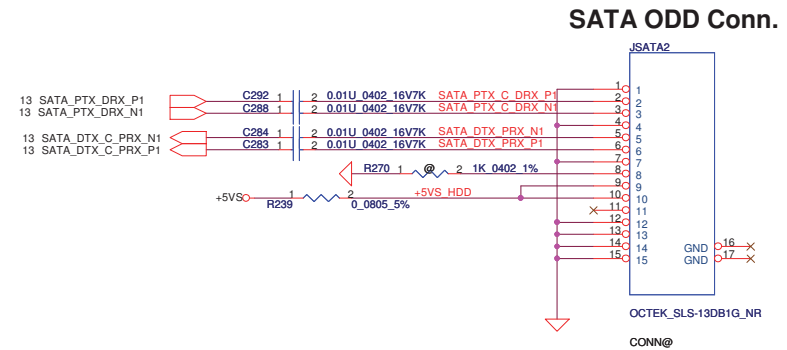
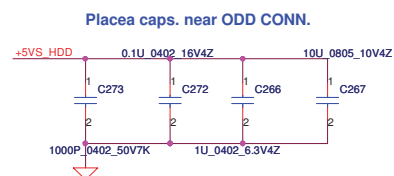
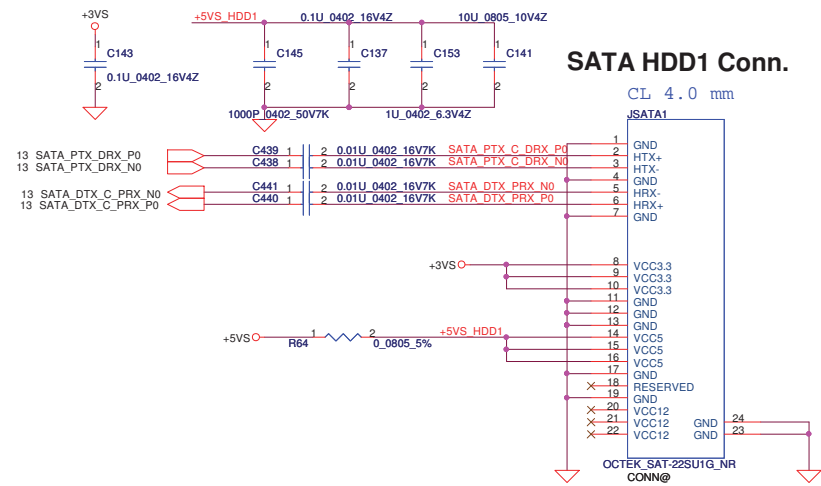
CRT Connector

Change to 0 ohm for Discrete

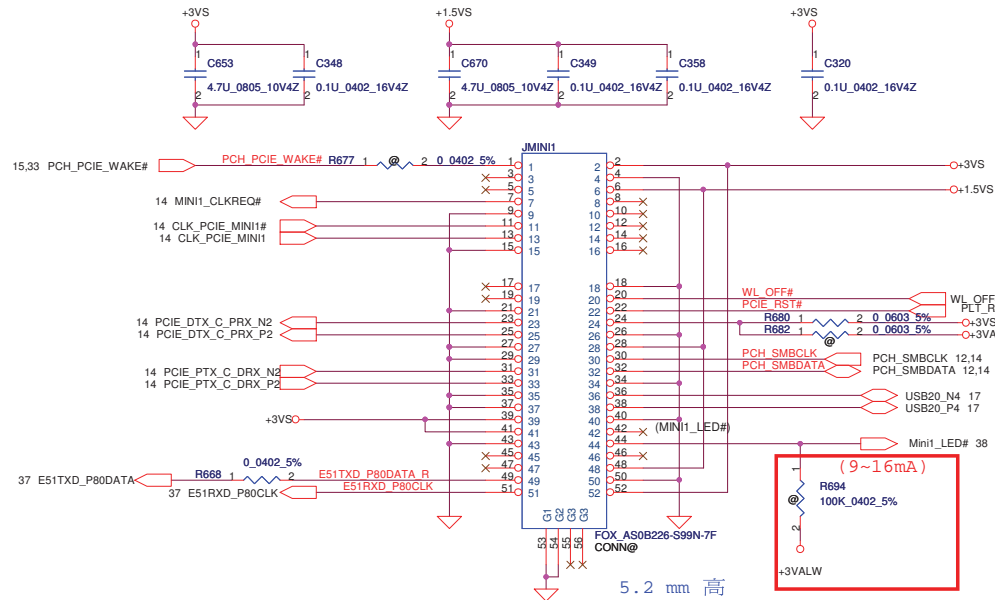


L	B1	DIS
H	B2	UMA

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				NALGO M/B LA-5681P Schematic		1.0
				Date	Friday, October 23, 2009	Sheet 29 of 60



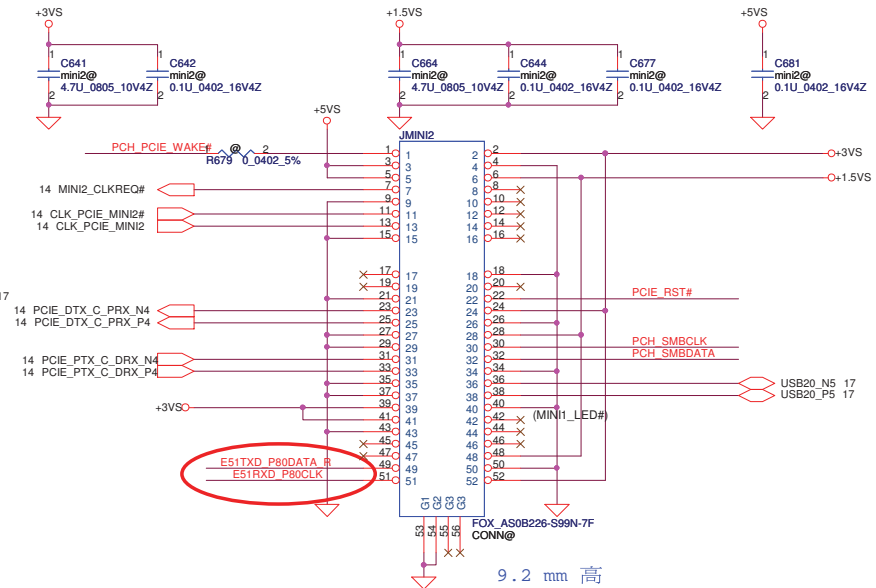
For Wireless LAN



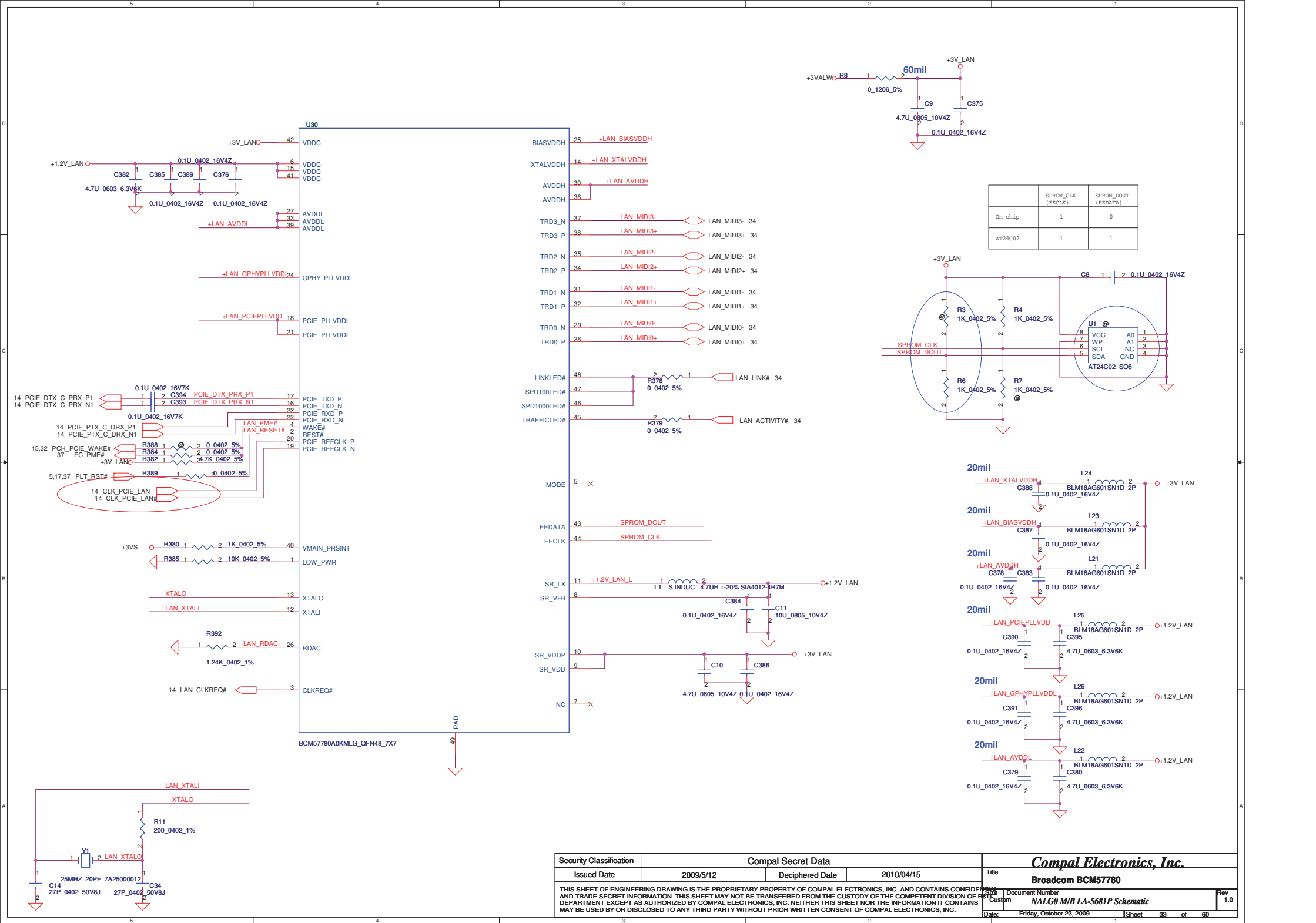
Mini Card Power Rating

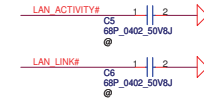
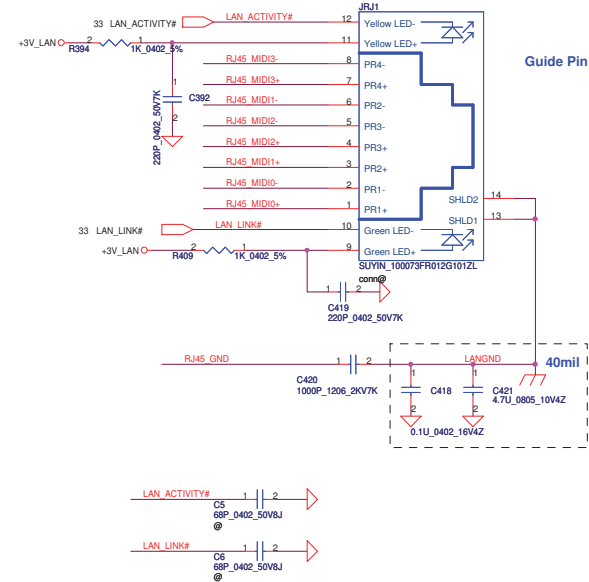
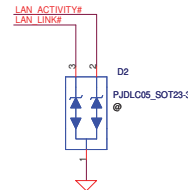
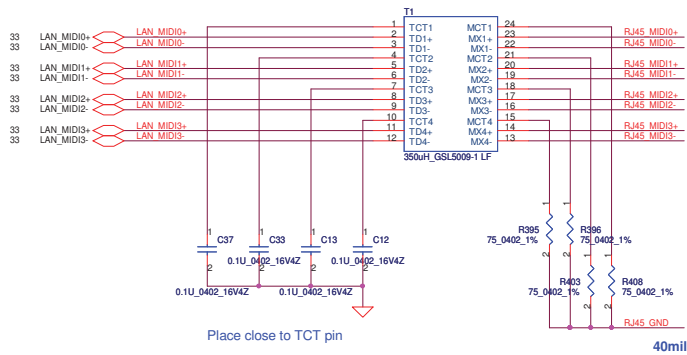
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

For TV-Tuner/HW MPEG



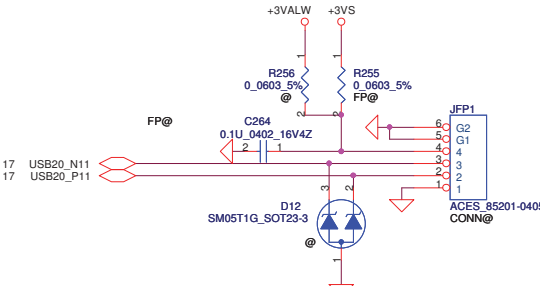
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Issued Date	2009/5/12	Deciphered Date	2007/12/25	Title	
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				NALG0 M/B LA-5681P Schematic	1.0
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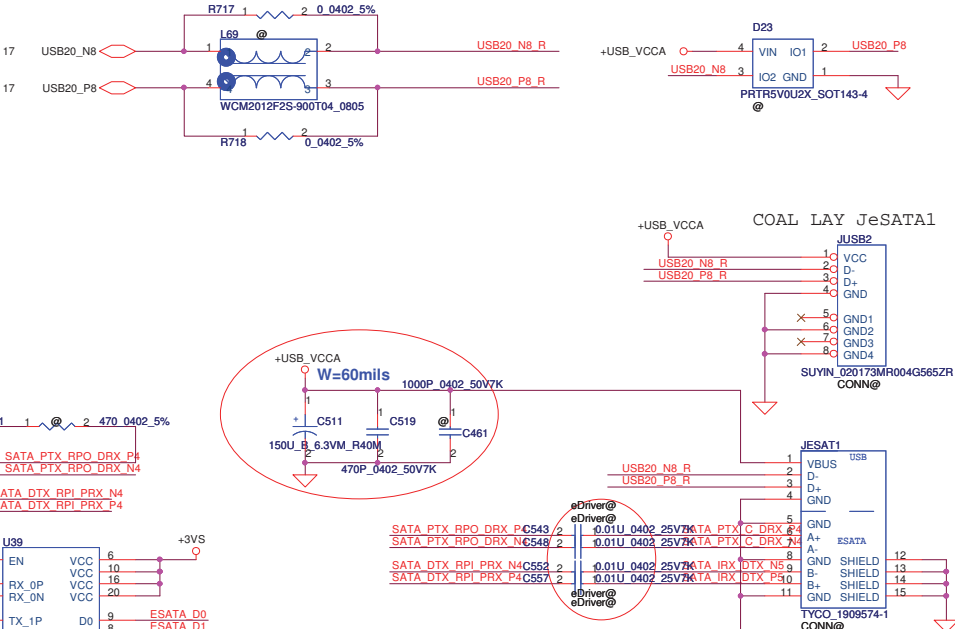
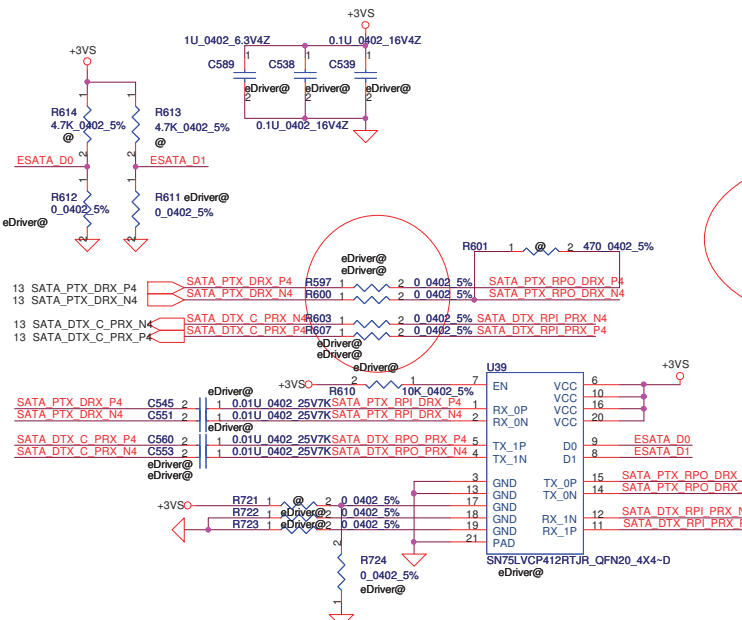
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Issued Date	2009/5/12	Deciphered Date	2010/04/15	Title	
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					NALG0 M/B LA-5681P Schematic
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				Rev	1.0

Finger Print Conn.

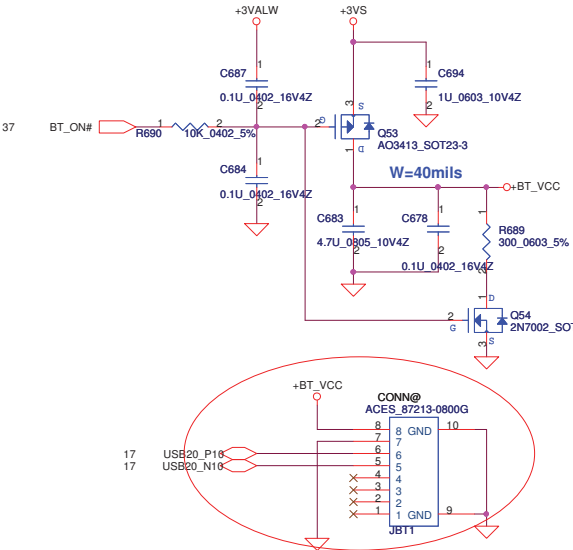


ESATA CONN

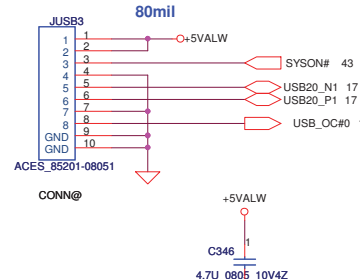
D0	D1	Function
0	0	default; CH0/CH1 ->0dB
0	1	CH0->2.5dB pre-emphasis;CH1->0dB
1	0	CH1->2.5dB pre-emphasis;CH0->0dB
1	1	CH0/CH1->2.5dB pre-emphasis



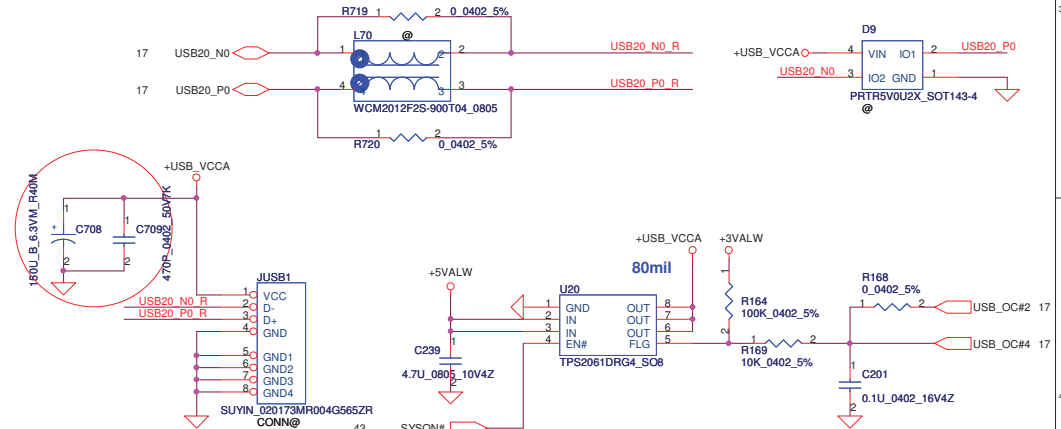
Bluetooth Conn.



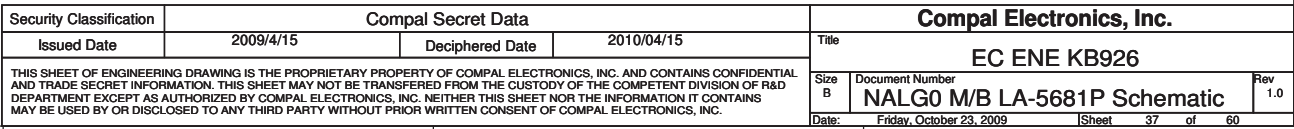
To USB/B Connector



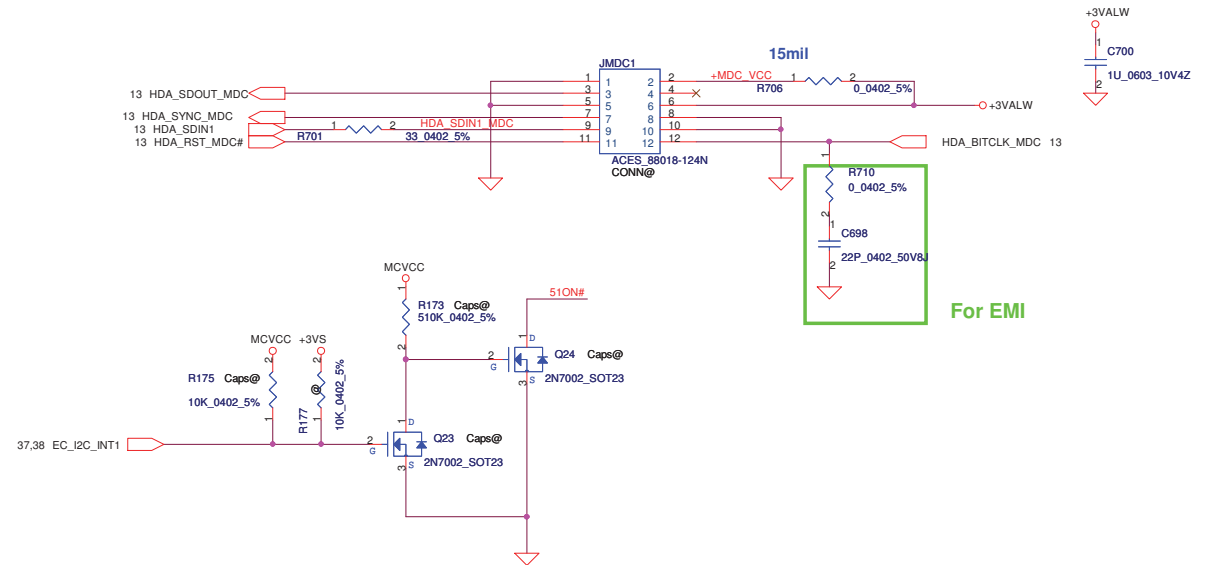
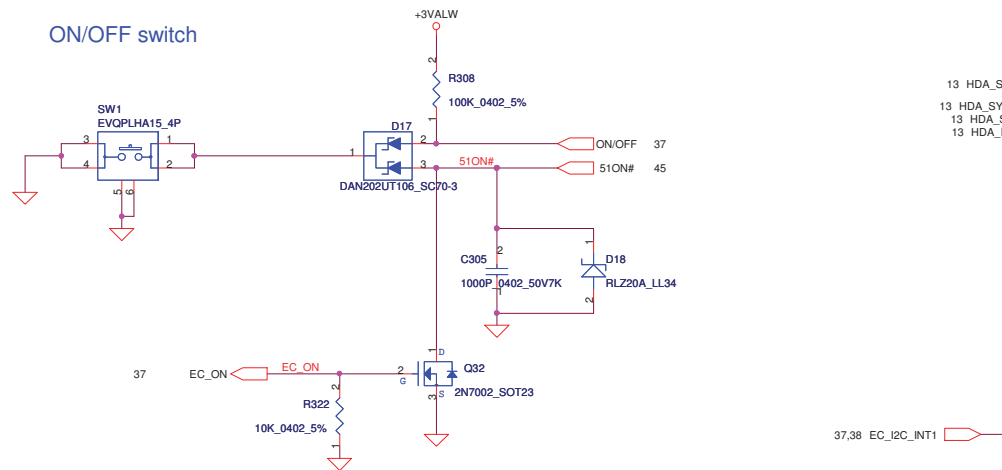
USB CONN.



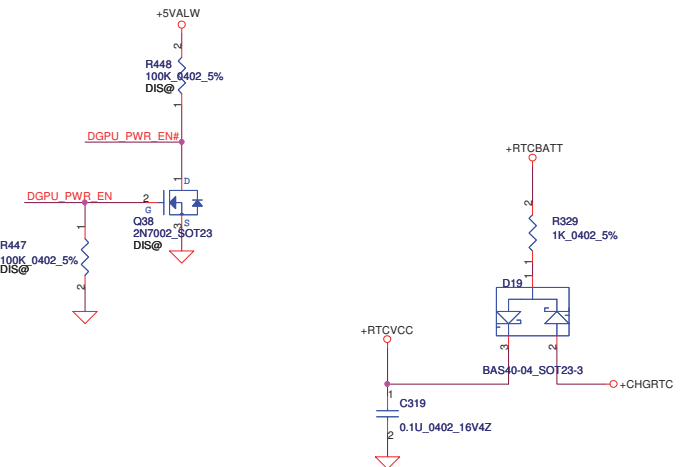
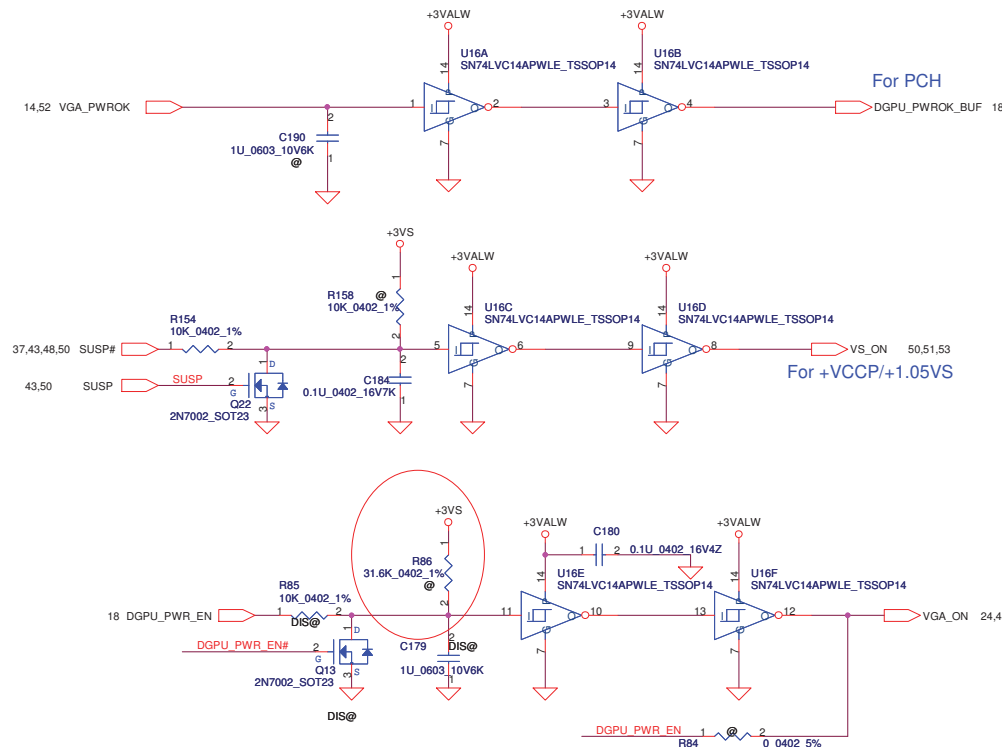
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2009/5/12	Deciphered Date		2009/12/31
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				NEW CARD & eSATA Connector	
				Document Number	
				Rev	
				1.0	
				NALGO M/B LA-5681P Schematic	
				Date: Friday, October 23, 2009	
				Drawn: ZF	



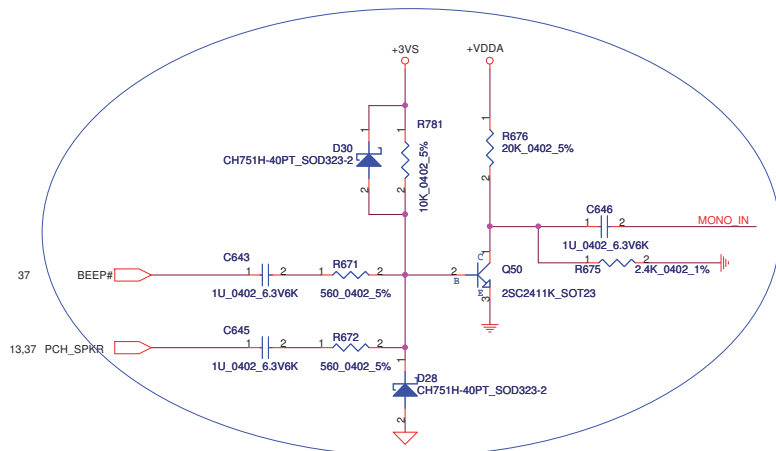
Power Button

HDA MDC Conn.

Power ON Circuit



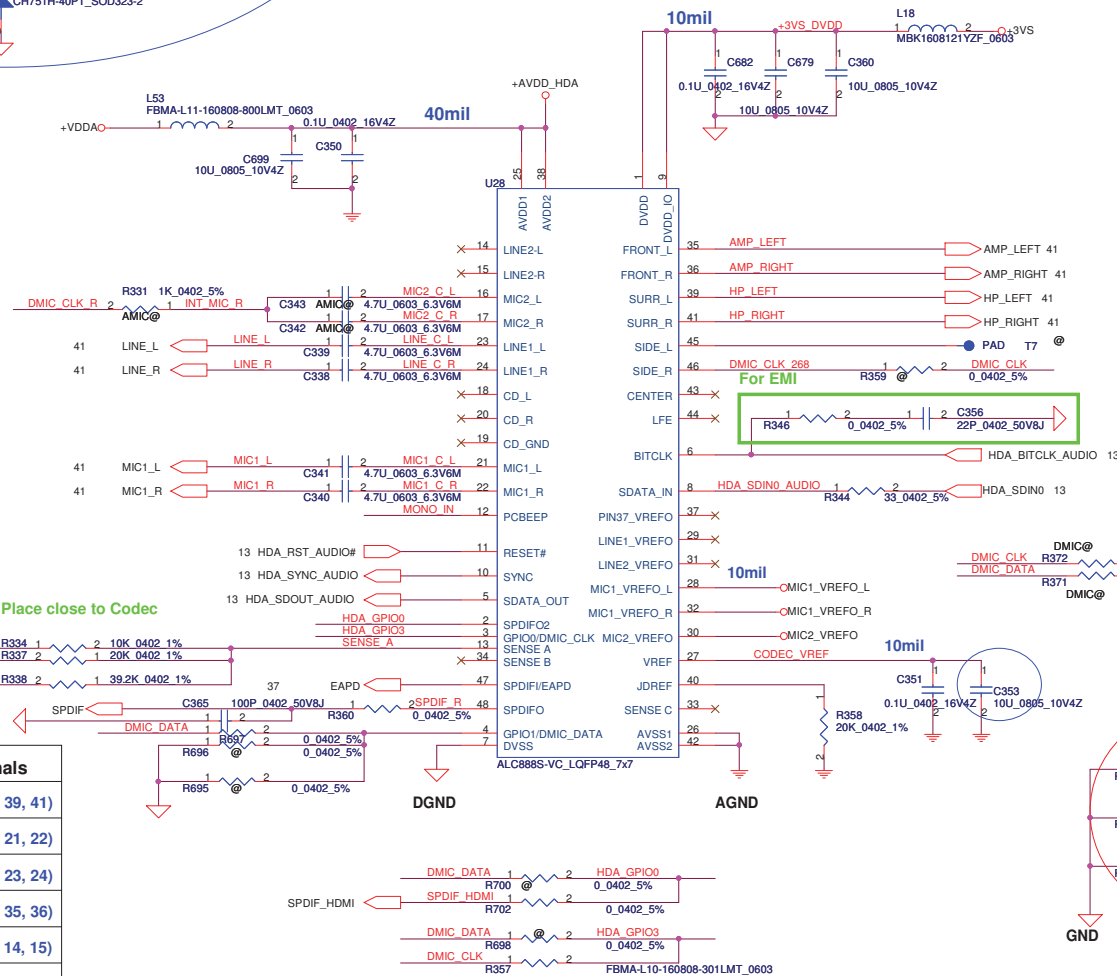
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2009/5/12	Deciphered Date	2009/12/31	Title	Power OK, Reset,RTC, CIR, MDC	
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BOM Option

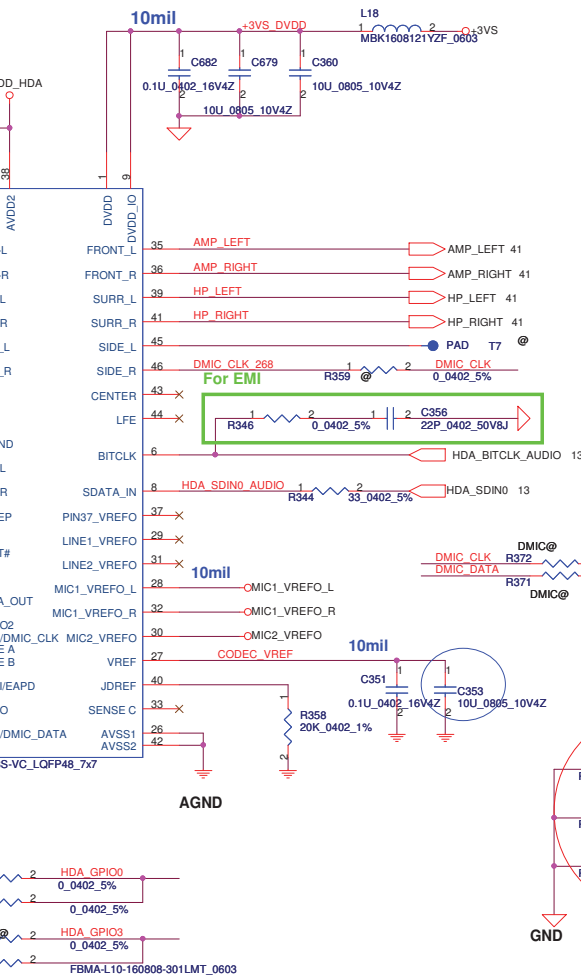
ALC268	268@
ALC888S-VB	888VB@
ALC888S-VC	888VC@

HD Audio Codec

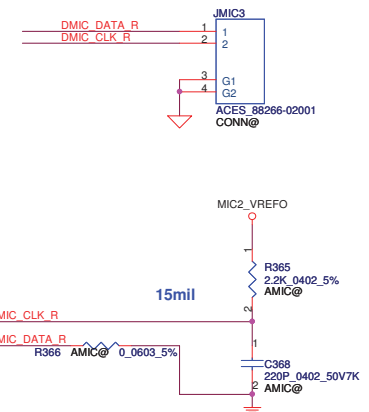


Place close to Codec

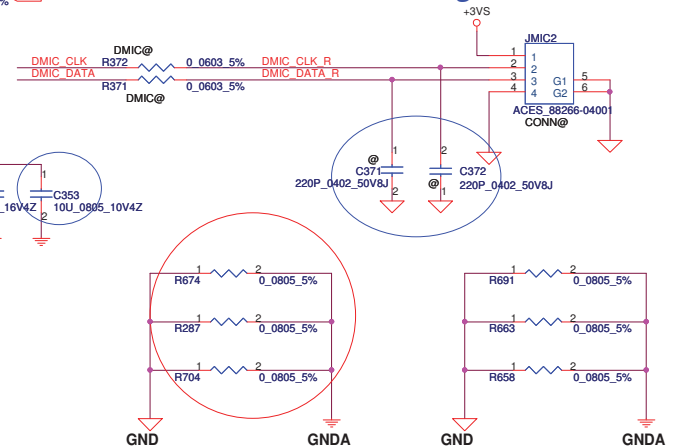
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



ANALOG MIC



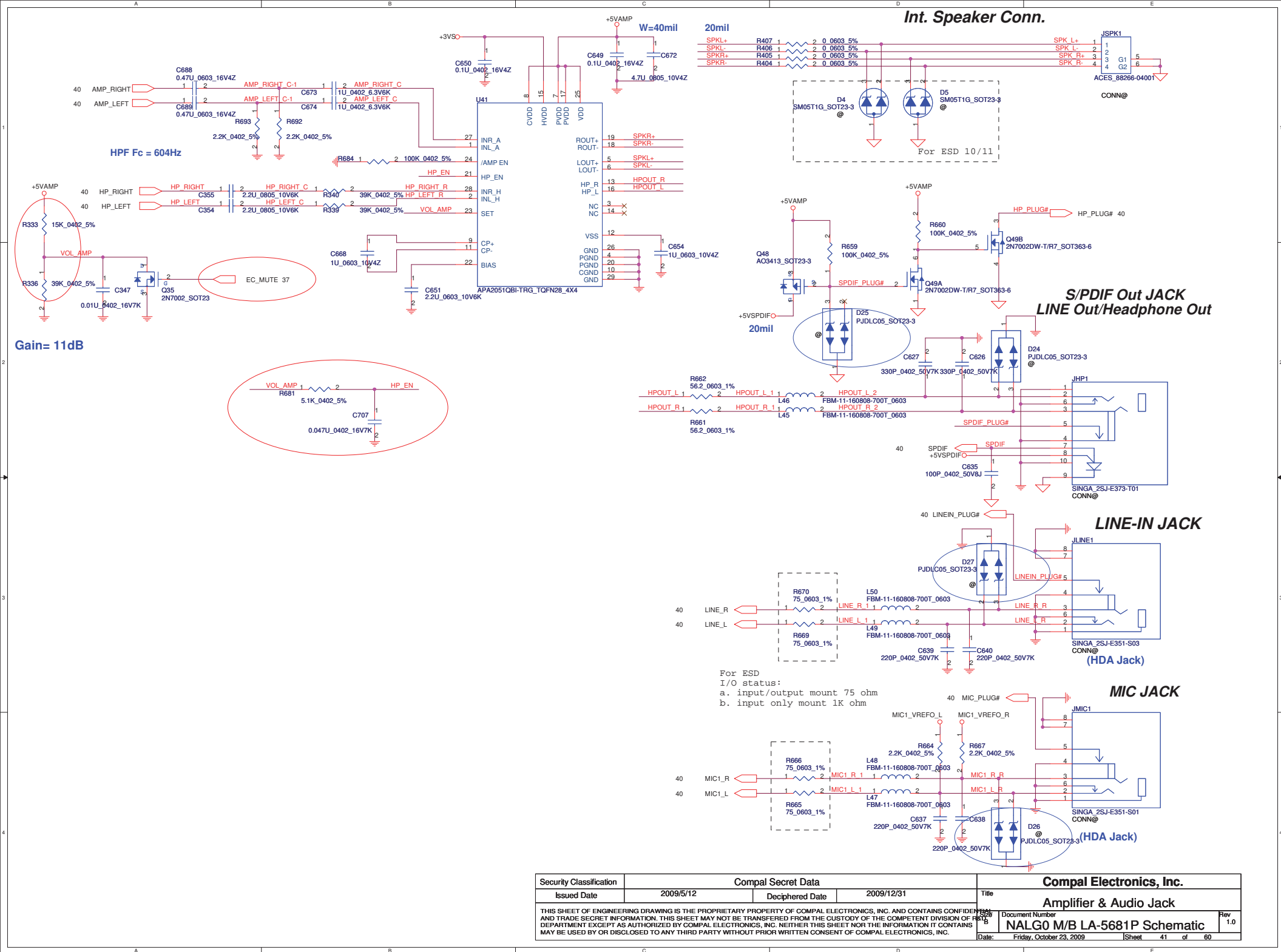
Digital MIC



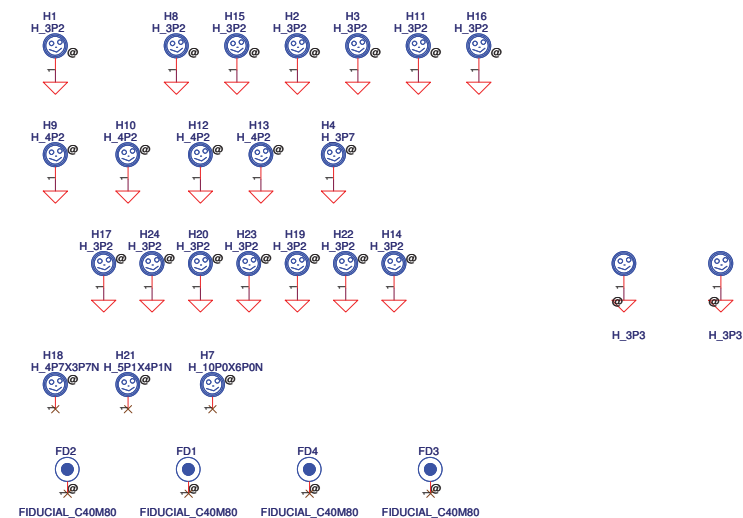
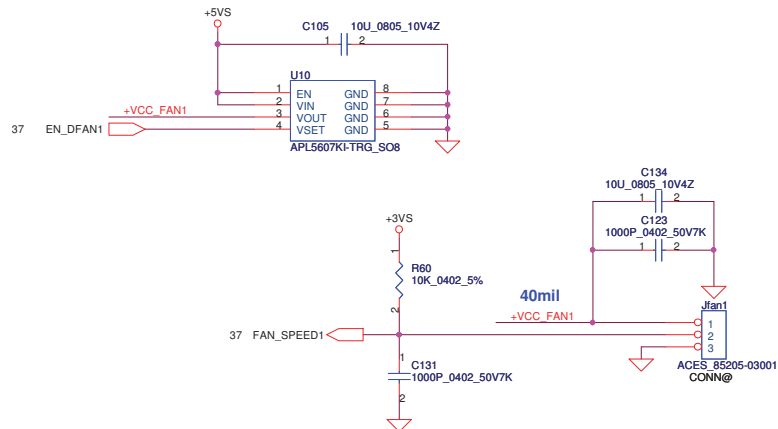
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2009/5/12		Deciphered Date		2009/12/31		Title			
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HD Audio Codec ALC888S-VC

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Sheet	40 of 60

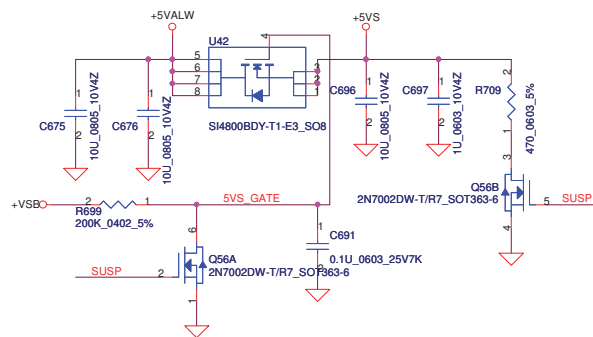


FAN1 Conn

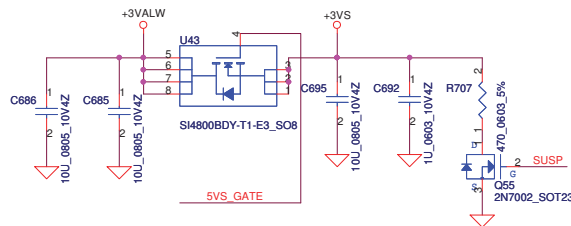


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				Date	Friday, October 23, 2009
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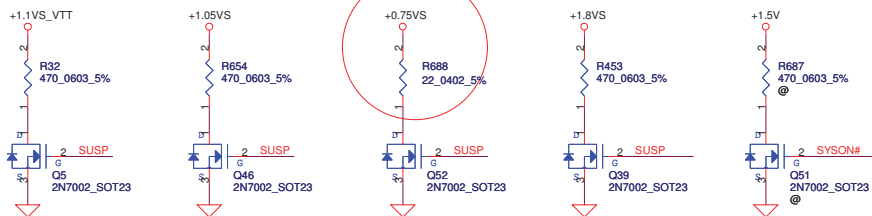
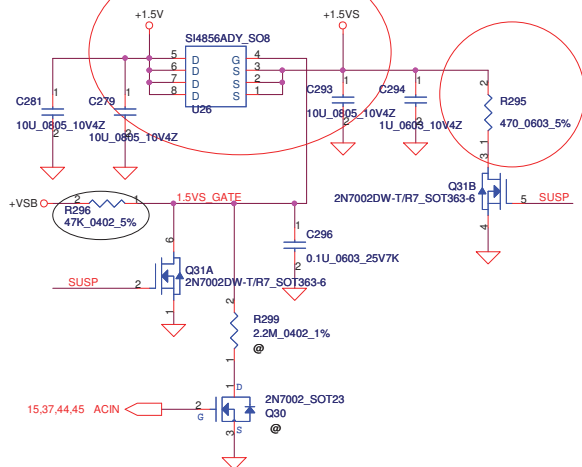
+5VALW TO +5VS



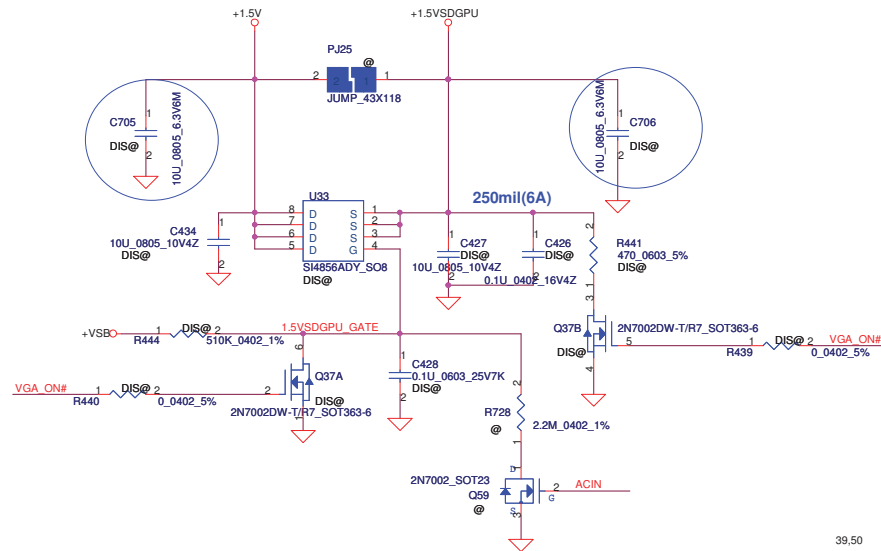
+3VALW TO +3VS



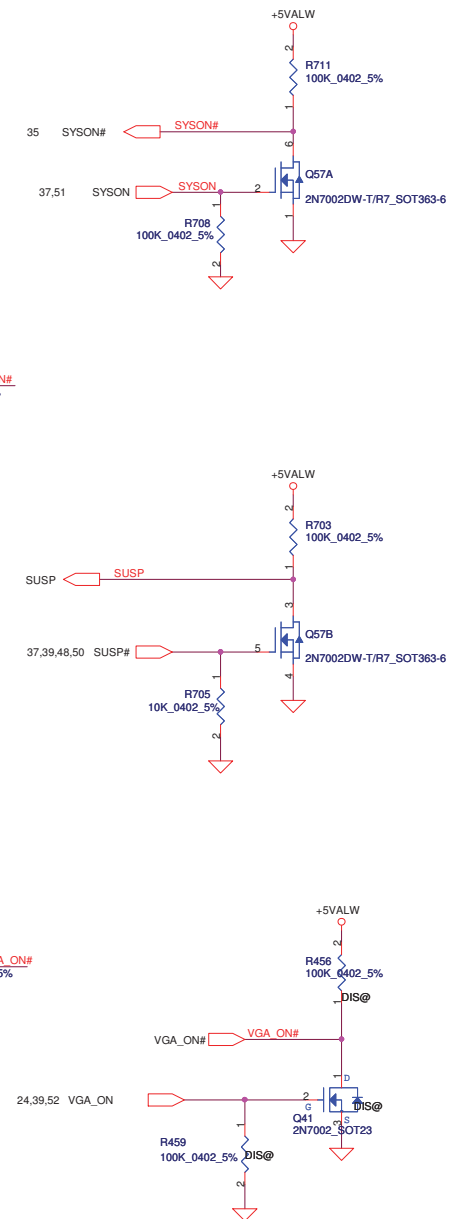
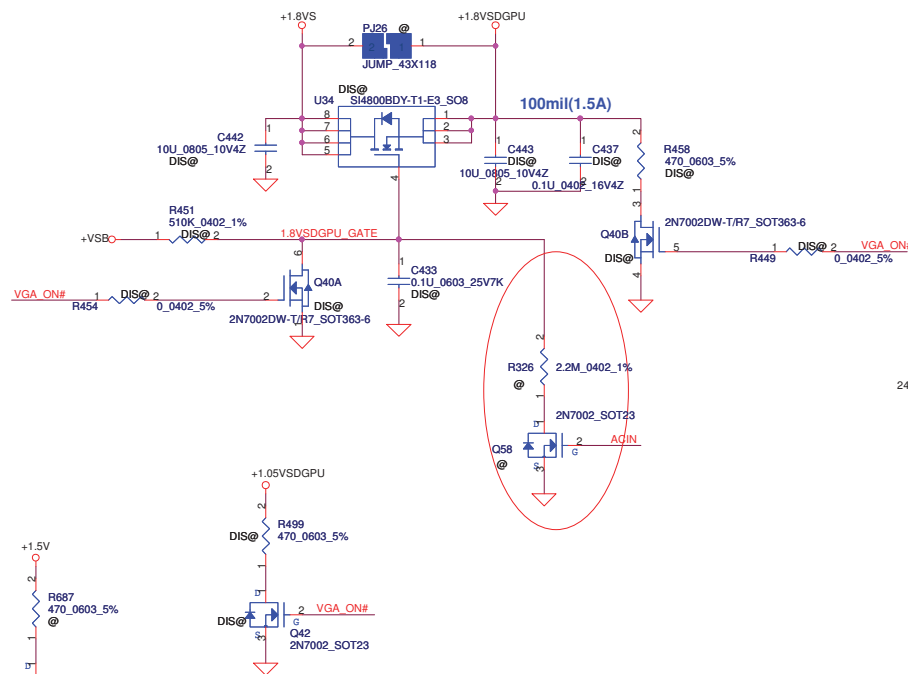
+1.5V to +1.5VS



+1.5V to +1.5VSDGPU Transfer

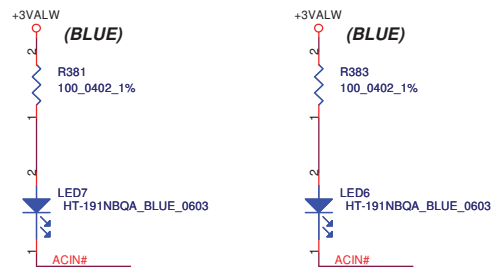


+1.8VS to +1.8VSDGPU Transfer

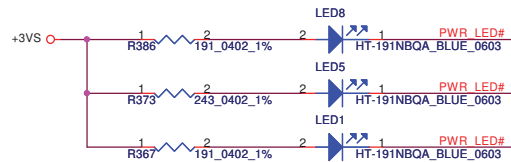


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				NALGO M/B LA-5681P Schematic	1.0
				Date: Friday, October 23, 2009	Sheet 43 of 60

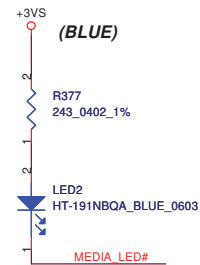
Enlightener LED



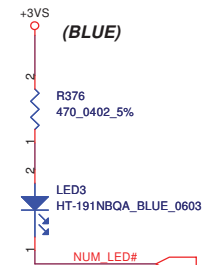
ON/OFF LED LEFT



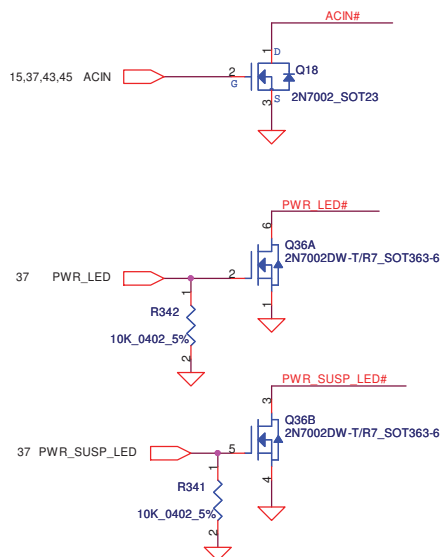
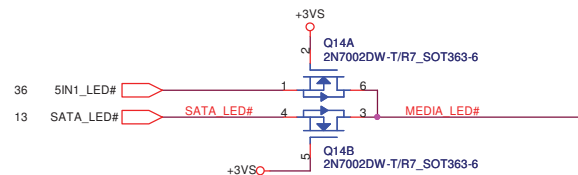
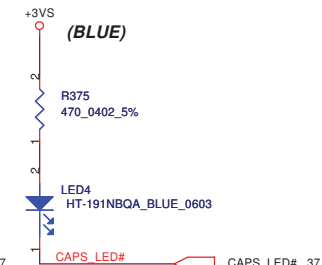
MEDIA_LED



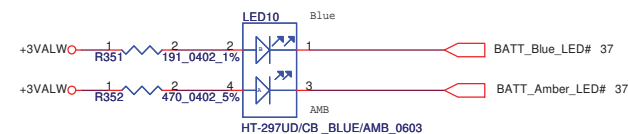
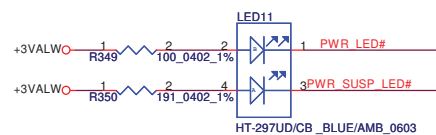
NUM_LED



CAPS_LED

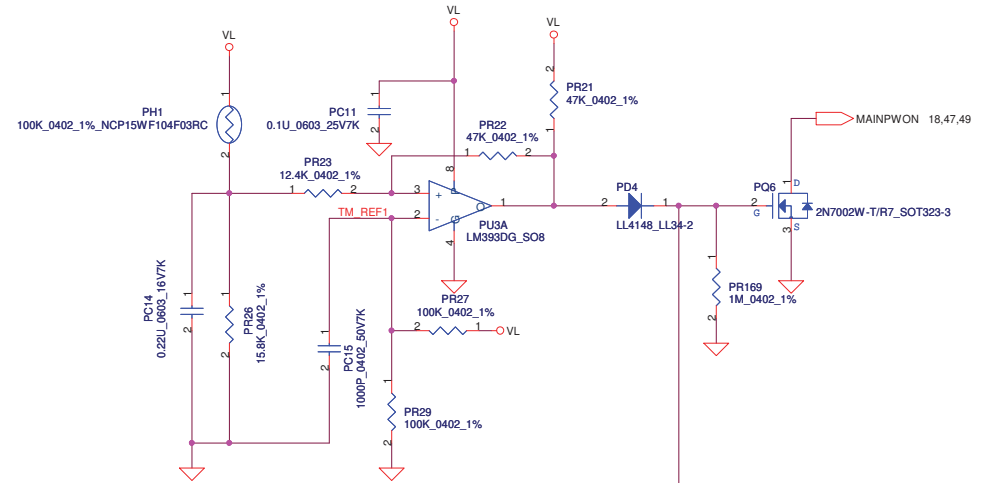
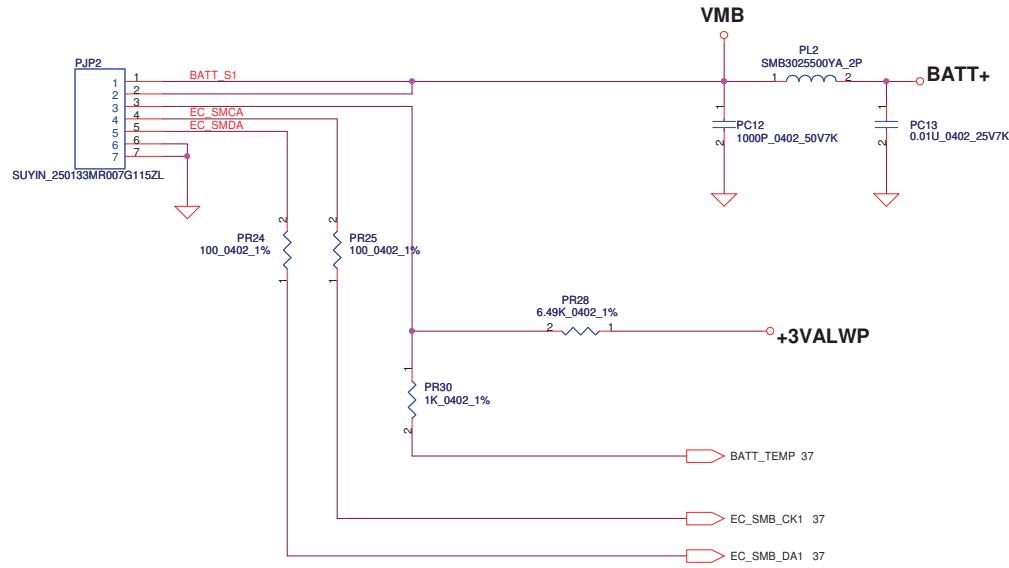


Compal Footprint

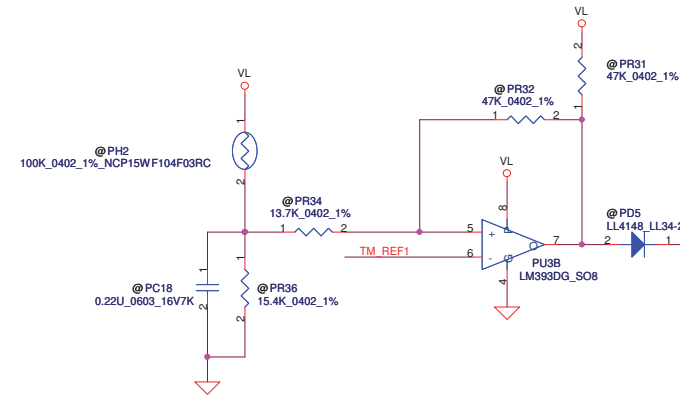
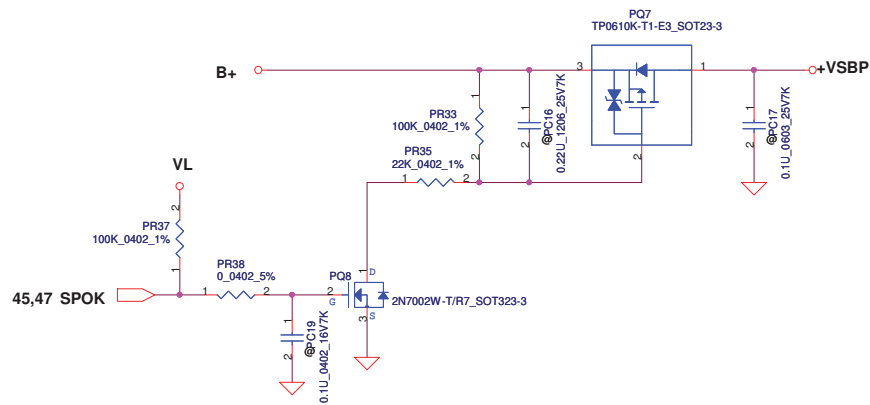


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								Size		Document Number	
		Custym		NALG0 M/B LA-5681P Schematic							
Date:		Friday, October 23, 2009		Sheet		44		of		60	

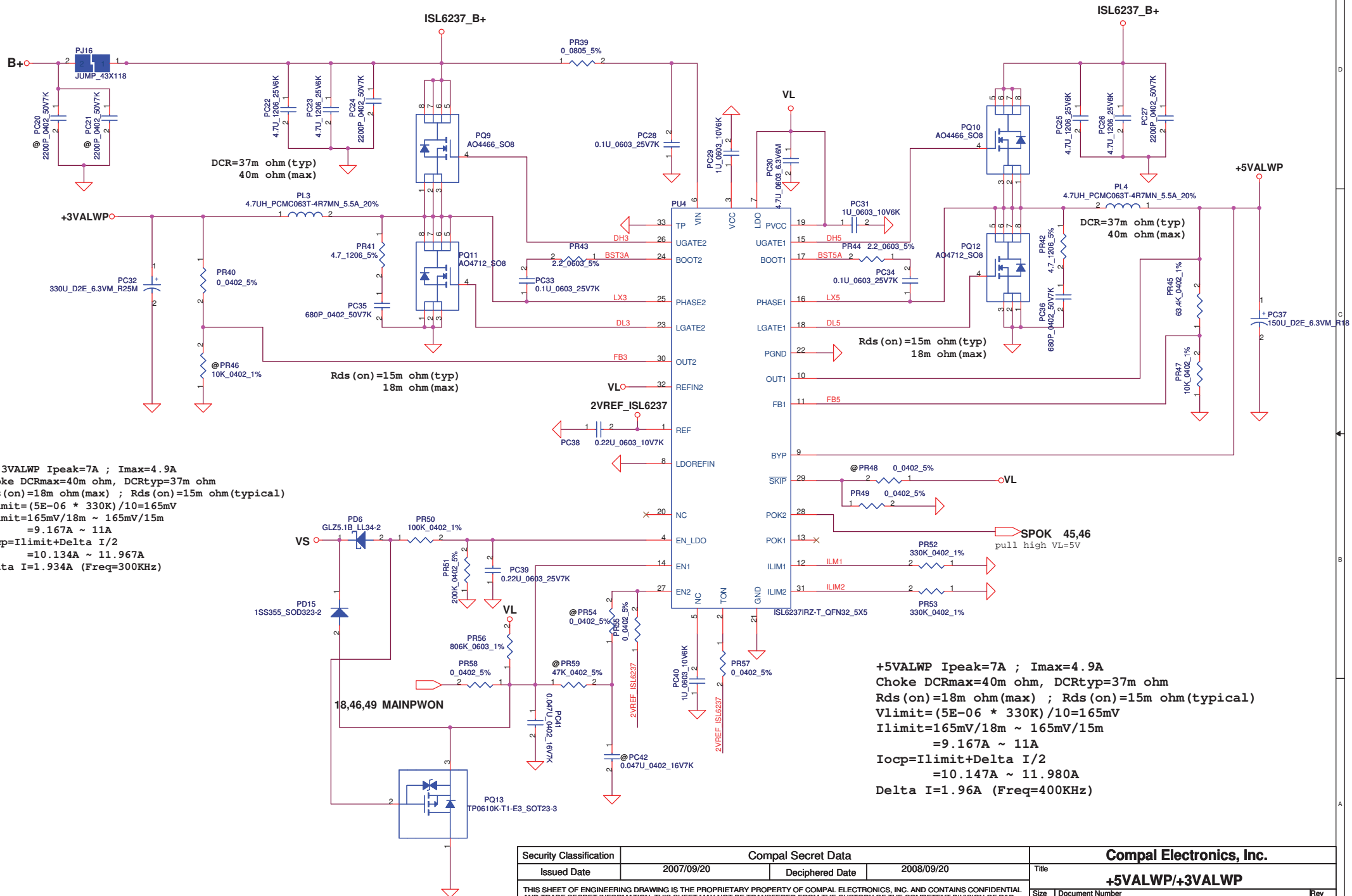
PH1 under CPU botten side :
CPU thermal protection at 92 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C



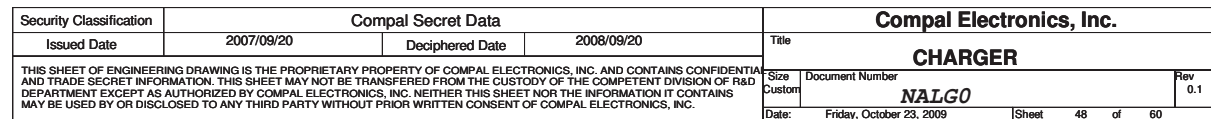
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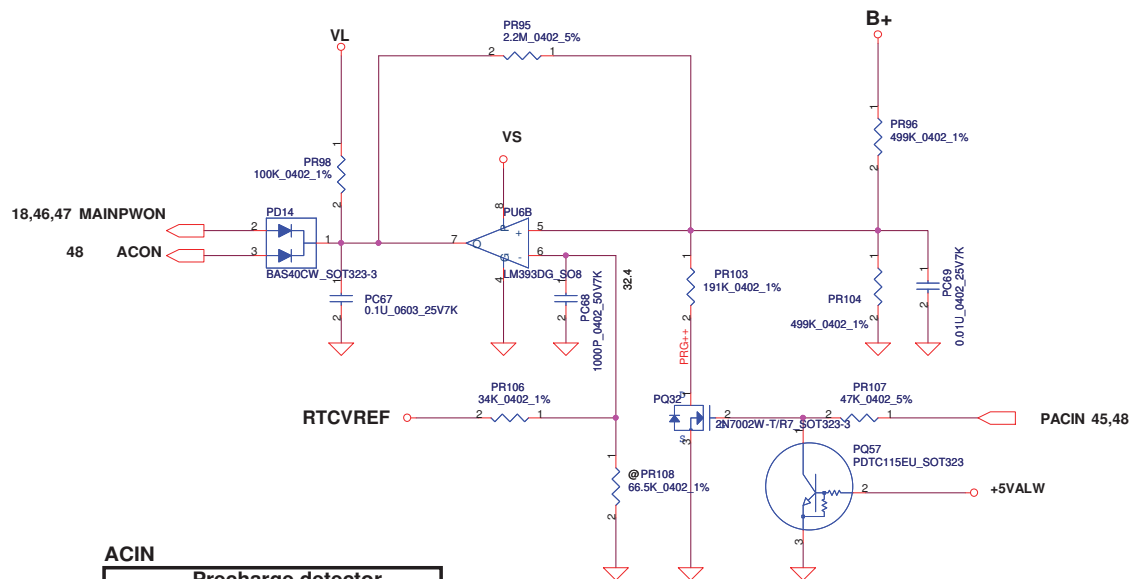
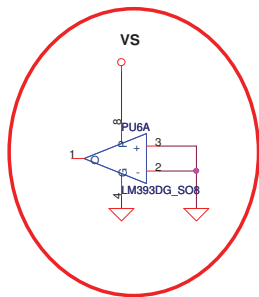


+3.3VALWP Ipeak=7A ; Imax=4.9A
Choke DCRmax=40m ohm, DCRtyp=37m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.134A ~ 11.967A
Delta I=1.934A (Freq=300KHz)

+5VALWP Ipeak=7A ; Imax=4.9A
Choke DCRmax=40m ohm, DCRtyp=37m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.147A ~ 11.980A
Delta I=1.96A (Freq=400KHz)

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$$\begin{aligned} \text{CP} &= 85\% \cdot I_{\text{ada}} ; \text{CP} = 4.07\text{A} \\ \text{CP} &= 85\% \cdot I_{\text{ada}} ; \text{CP} = 2.91\text{A} \end{aligned}$$




ACIN

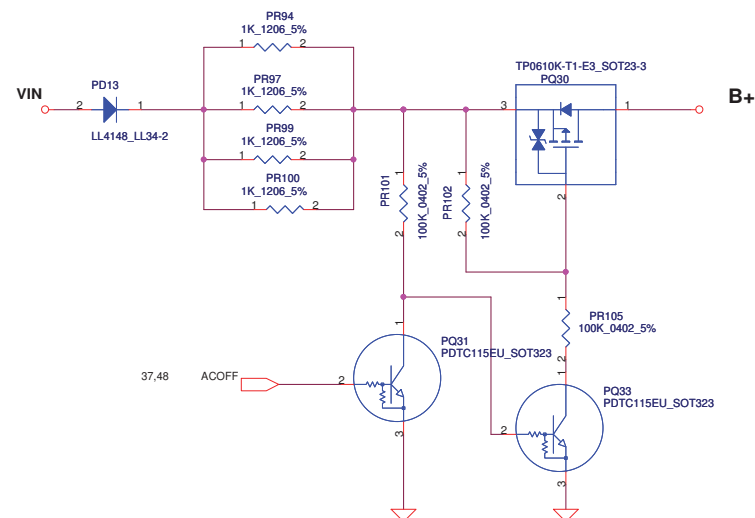
Precharge detector

	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

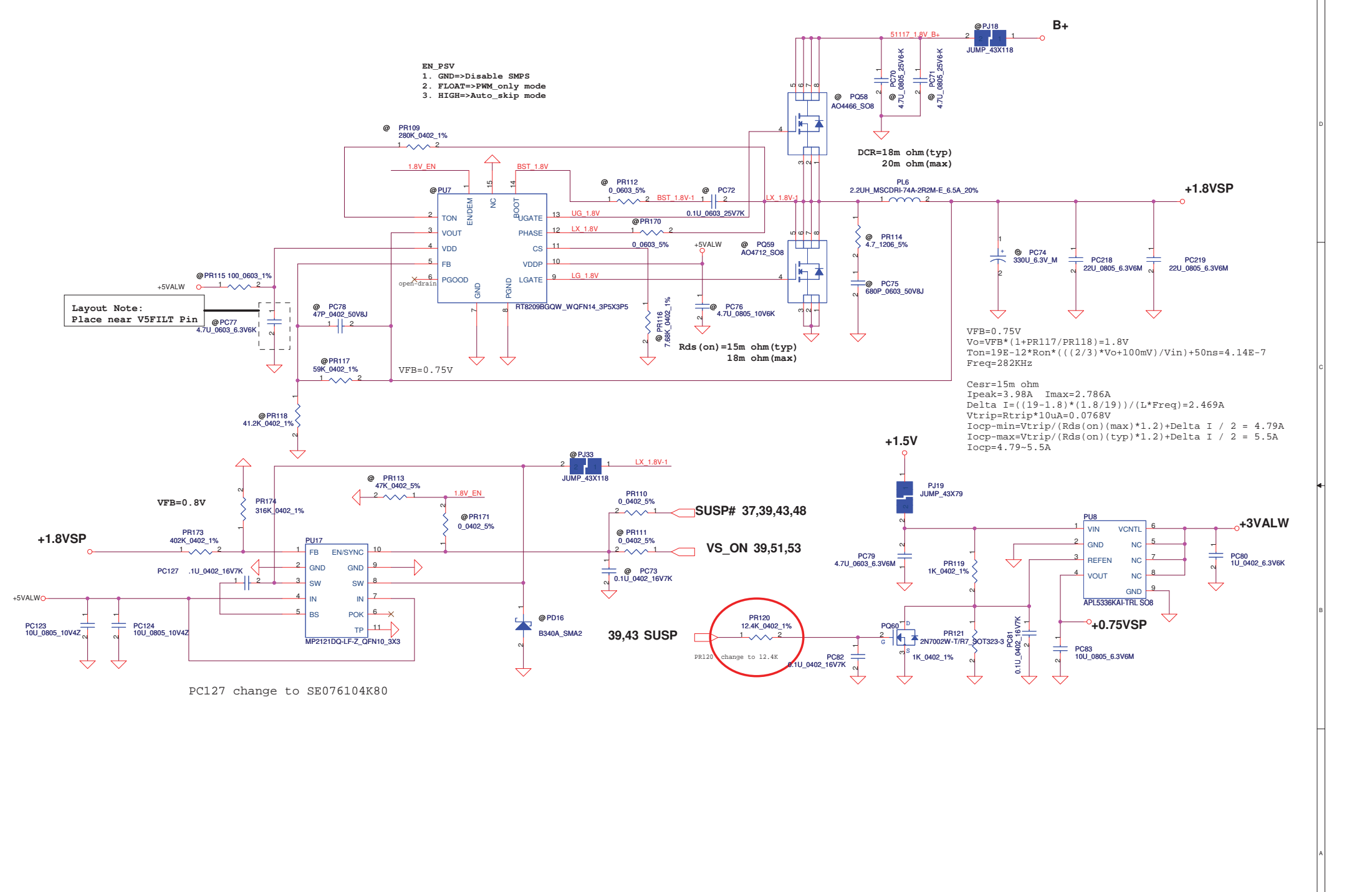
BATT ONLY

Precharge detector

	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



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EN_PSV
1. GND=>Disable SMPS
2. FLOAT=>PWM_only mode
3. HIGH=>Auto_skip mode

Layout Note:
Place near V5FILT Pin

VFB=0.75V
 $V_o = VFB * (1 + PR117 / PR118) = 1.8V$
 $Ton = 19E-12 * Ron * ((2/3) * V_o + 100mV) / Vin + 50ns = 4.14E-7$
Freq=282KHz

Cesr=15m ohm
Ipeak=3.98A Imax=2.786A
 $\Delta I = ((19-1.8) * (1.8/19)) / (L * Freq) = 2.469A$
 $Vtrip = Rtrip * 10uA = 0.0768V$
 $Iocp_min = Vtrip / (Rds(on)(max) * 1.2) + \Delta I / 2 = 4.79A$
 $Iocp_max = Vtrip / (Rds(on)(typ) * 1.2) + \Delta I / 2 = 5.5A$
 $Iocp = 4.79 \sim 5.5A$

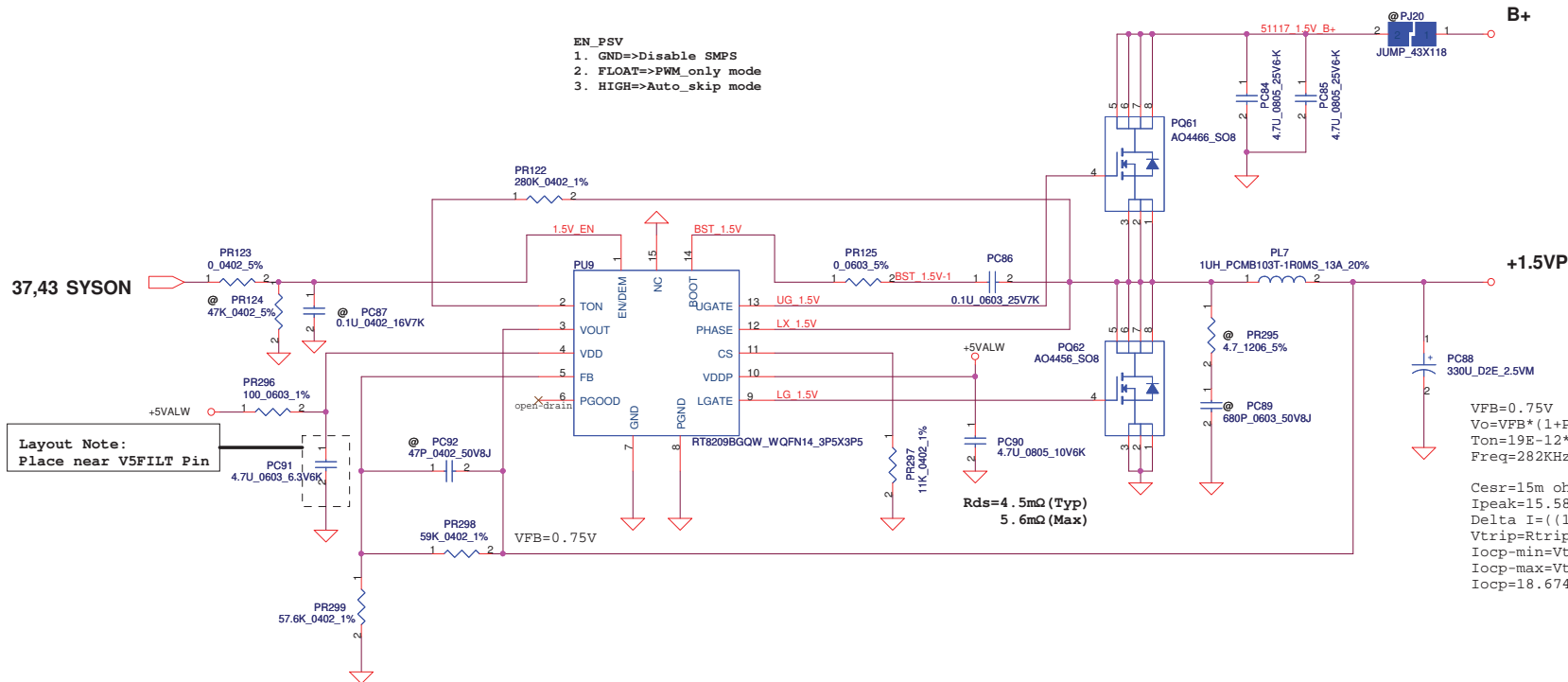
PC127 change to SE076104K80

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EN_PSV
1. GND=>Disable SMPS
2. FLOAT=>PWM_only mode
3. HIGH=>Auto_skip mode

37,43 SYSON

Layout Note:
Place near V5FILT Pin



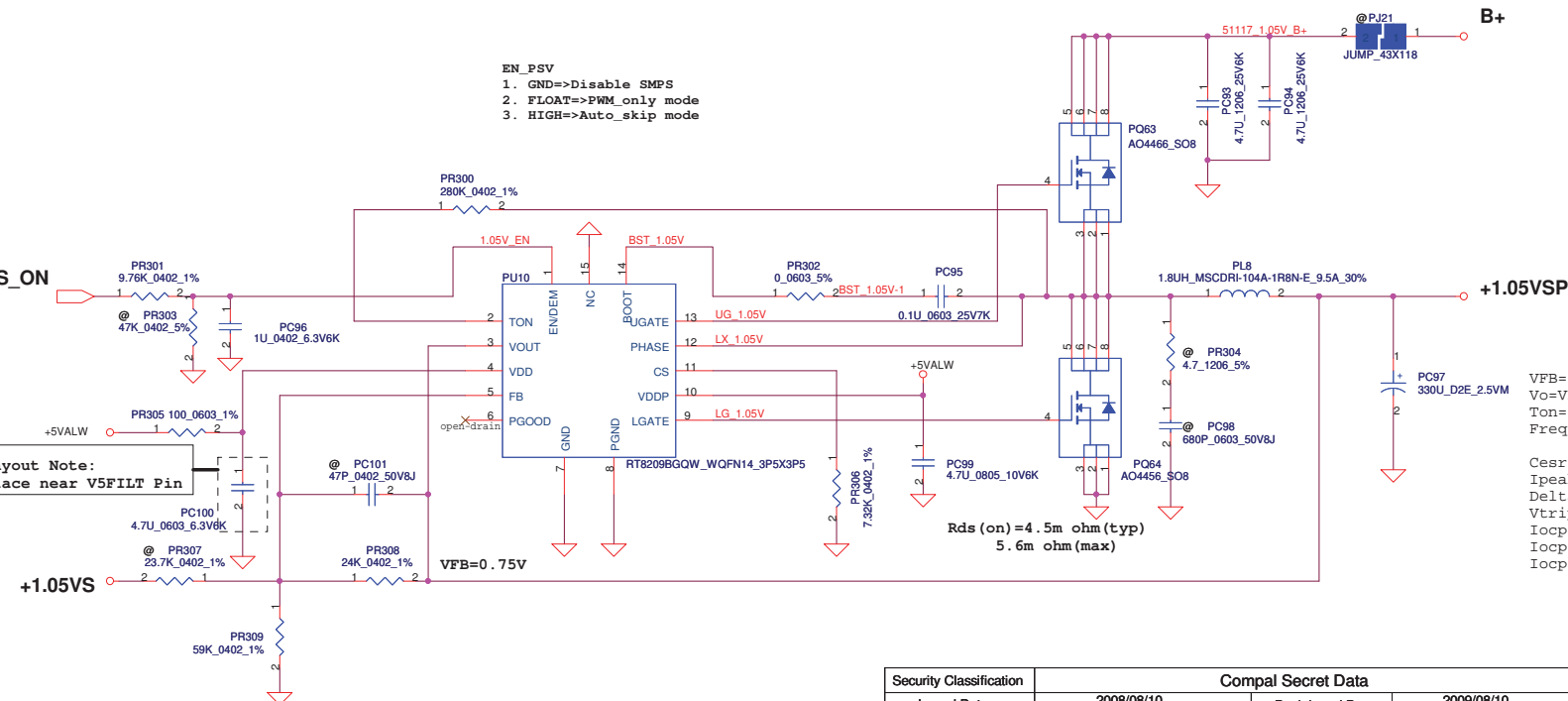
VFB=0.75V
Vo=VFB*(1+PR298/PR299)=1.52V
Ton=19E-12*Ron*((2/3)*Vo+100mV)/Vin+50ns=3.8E-7
Freq=282KHz(min) , 300KHz(typ)

Cesr=15m ohm
Ipeak=15.58A Imax=10.906A
Delta I=((19-1.5)*(1.5/19))/(L*Freq)=4.61A
Vtrip=Rtrip*10uA=0.11V
Iocp-min=Vtrip/(Rds(on)(max)*1.2)+Delta I / 2= 18.674A
Iocp-max=Vtrip/(Rds(on)(typ)*1.2)+Delta I / 2=22.675A
Iocp=18.674~22.675A

EN_PSV
1. GND=>Disable SMPS
2. FLOAT=>PWM_only mode
3. HIGH=>Auto_skip mode

53 VS_ON

Layout Note:
Place near V5FILT Pin



VFB=0.75V
Vo=VFB*(1+PR308/PR309)=1.05V
Ton=19E-12*Ron*((2/3)*Vo+100mV)/Vin+50ns=2.74E-07
Freq=282KHz , 300KHz(typ)

Cesr=15m ohm
Ipeak=10.9A Imax=7.63A
Delta I=((19-1.05)*(1.05/19))/(L*Freq)=1.837A
Vtrip=Rtrip*10uA=0.0732V
Iocp-min=Vtrip/(Rds(on)(max)*1.2)+Delta I / 2= 11.81A
Iocp-max=Vtrip/(Rds(on)(typ)*1.2)+Delta I / 2=14.47A
Iocp=11.81~14.47A

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				Deciphered Date				1.5VP / 1.05VSP			
				2009/08/10				Size			
								Document Number			
								Custom			
								NALGO			
								Rev			
								0.1			
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Layout Note:
Place near high-side MOS Drain
and low-side MOS Source

Layout Note:
Close IC

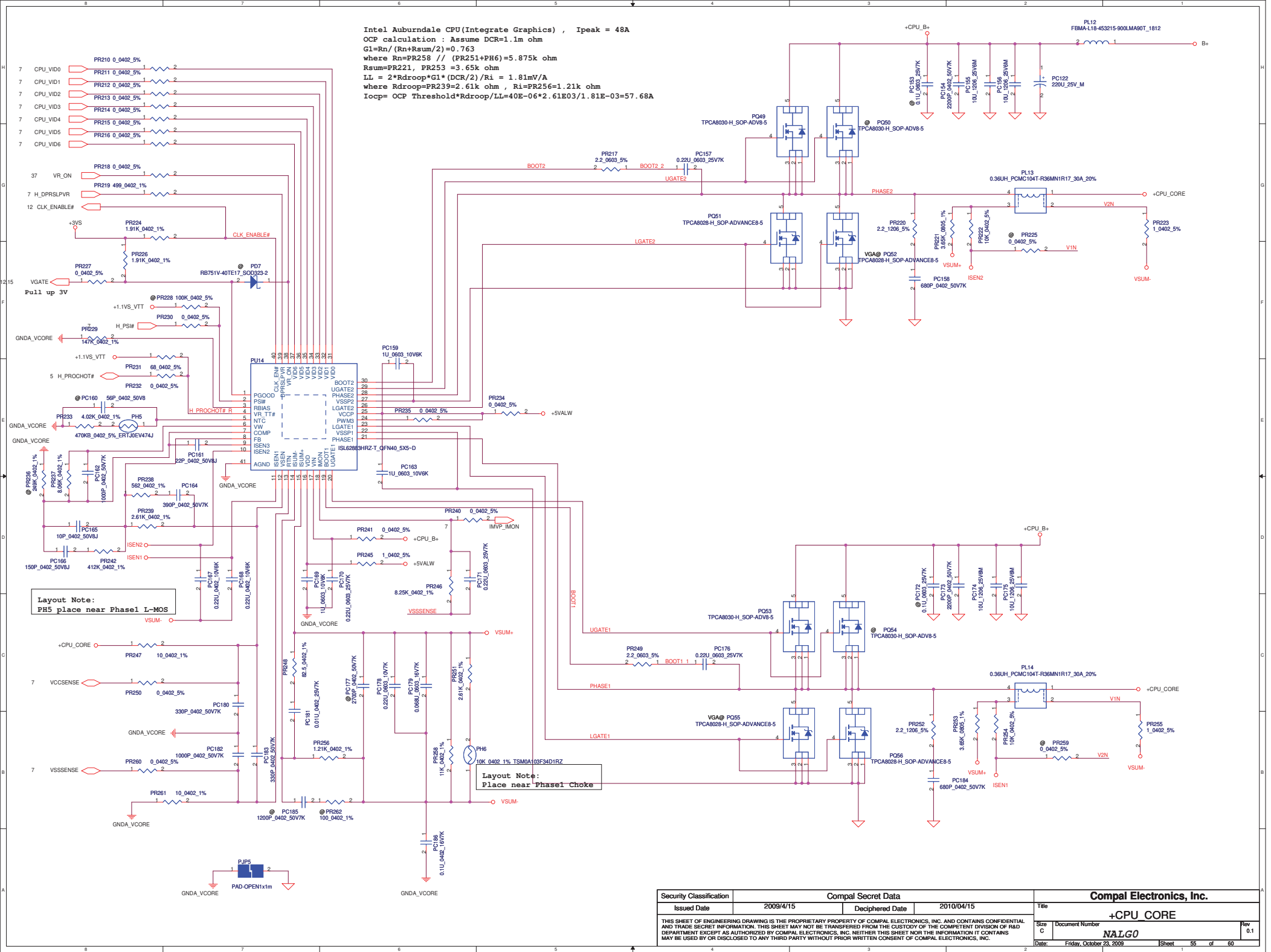
Layout Note:
Close IC
單獨拉回不搭Pin15

Material Note:
330uF/9 mΩ, number
are 3, Power 1, HW 2

+1.1VS_VTT
Ipeak=18.06A
Imax=12.642A
Delta I / 2 = 2.176A , Freq=230K Hz
Iocp(min)=Ipeak + Delta I / 2 = 20.236A
Rsen=Iocp(min)*1.2*Rds(on)(max)/ISEN(min)=2.05K ohm
ISEN(min)=19uA , Rds(on)=3.2m ohm(max) , 2.3m ohm(typ)
Iocp(max)=ISEN(min)*Rsen/(1.2*Rds(on)(typ))=28.225A
Iocp=20.236~28.225A

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Intel Auburndale CPU(Integrate Graphics) , Ipeak = 48A
 OCP calculation : Assume DCR=1.1m ohm
 $G1=Rn/(Rn+Rsum/2)=0.763$
 where $Rn=PR258 // (PR251+PH6)=5.875k\ ohm$
 $Rsum=PR221, PR253 =3.65k\ ohm$
 $LL = 2 * Rdroop * G1 * (DCR/2) / Ri = 1.81mV/A$
 where $Rdroop=PR239=2.61k\ ohm$, $Ri=PR256=1.21k\ ohm$
 $Iocp= OCP\ Threshold * Rdroop / LL = 40E-06 * 2.61E03 / 1.81E-03 = 57.68A$



Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Modify chager circuit	design change	0.1	48	Change PR60 to SD000001F00(0.02_2512_1%)	09/06/23	EVT
2	Modify 1.8V V5FILT PIN	Avoid 2'nd source RT8209B can no power on	0.1	50	Cahnge PR115 to SD014100080 (S RES 1/10W 100 +-1% 0603)	09/07/21	DVT
3	Modify 1.5V V5FILT PIN	Avoid 2'nd source RT8209B can no power on	0.1	51	Cahnge PC77 to SE107475K80 (S CER CAP 4.7U 6.3V K X5R 0603)	09/07/21	DVT
4	Modify 1.05V V5FILT PIN	Avoid 2'nd source RT8209B can no power on	0.1	51	Cahnge PR296 to SD014100080 (S RES 1/10W 100 +-1% 0603)	09/07/21	DVT
5	Modify VGA_COREP circuit	design change	0.1	52	Cahnge PC91 to SE107475K80 (S CER CAP 4.7U 6.3V K X5R 0603)	09/07/21	DVT
6	Modify +1.1VS_VTTP circuit	design change	0.1	53	Cahnge PR305 to SD014100080 (S RES 1/10W 100 +-1% 0603)	09/07/21	DVT
7	Modify OTP circuit	Link right component	0.1	46	Cahnge PC100 to SE107475K80 (S CER CAP 4.7U 6.3V K X5R 0603)	09/07/21	DVT
8	Modify 5V/3V circuit	Delete component	0.1	47	Cahnge PR149 to SD028000080 (S RES 1/16W 0 +-5% 0402)	09/06/23	EVT
9	Modify 1.1VSDGPU circuit	design change	0.1	52	Cahnge PR150 to SD034100A80 (S RES 1/16W 10 +-1% 0402)	09/06/23	EVT
10	Modify chager circuit	design change	0.1	48	Cahnge PR139 to SD028000080 (S RES 1/16W 0 +-5% 0402)	09/06/23	EVT
11	Modify VGA_COREP circuit	design change(Voltage Level)	0.1	52	Cahnge PR168 to SD034100A80 (S RES 1/16W 10 +-1% 0402)	09/06/23	EVT
12	Modify VGA_COREP circuit	design change(Voltage Level)	0.1	52	Add PH1 to SL210031F00 (S THERM_ 100K +-1% TH11-4H104FT 0603)	09/06/25	EVT
13	Modify OTP circuit	design change	0.2	46	Delete PC42 to SE076473K80 (S CER CAP .047U 16V K X7R 0402)	09/06/25	EVT
14	Modify 1.5VP circuit	design change	0.2	51	Change PU16, PR165, PR166, PR167, PC211, PC212, PC213, PC214, PC215, PC216 BOM structure to VGA@	09/06/26	EVT
15	Modify VGA_COREP circuit	design change	0.2	52	Change PR78 to SD012200D80(S RES 1/2W 0.02 +-1% 1206)	09/06/26	EVT
16	Modify +1.1VS_VTTP circuit	design change	0.2	53	Cahnge PR151 to SD034240180 (S RES 1/16W 2.4K +-1% 0402)	09/06/30	EVT
17	Modify CPU circuit	design change	0.2	55	Cahnge PR156 to SD000002680 (S RES 1/16W 6.98K +-1% 0402)	09/06/30	EVT
18	Modify CPU circuit	design change	0.2	55	Cahnge PR154 to SD034237280 (S RES 1/16W 23.7K +-1% 0402)	09/06/30	EVT
19	Modify CPU circuit	design change	0.2	55	Cahnge PR159 to SD034130280 (S RES 1/16W 13K +-1% 0402)	09/06/30	EVT
20	Modify +1.1VS_VTTP circuit	design change	0.2	53	Cahnge PQ6 to SB000006800 (S TR 2N7002W T/R7 1N SOT-323)	09/07/13	DVT
21	Modify CPU circuit	design change	0.2	55	Add PR169 to SD034100480 (S RES 1/16W 1M +-1% 0402)	09/07/13	DVT
22	Modify chager circuit	design change	0.2	48	Change PL7 to SH000009U00(S COIL 1UH +-20% FDUE1040D-1R0M=P3 21.3A)	09/07/20	DVT
23	Modify 1.1VSDGPU circuit	design change	0.2	52	Cahnge PR153 to SD034576280 (S RES 1/16W 57.6K +-1% 0402)	09/07/20	DVT
					Cahnge PQ35 to SB000006L00 (S TR TPCA8028-H 1N SOP ADVANCE)	09/07/20	DVT
					Cahnge PQ36 to SB000006L00 (S TR TPCA8028-H 1N SOP ADVANCE)	09/07/20	DVT
					Cahnge PC107 to SF000002000 (S ELE CAP 330U 6.3V M 6.3X5.9 LESR15M VU)	09/07/20	DVT
					Cahnge PC74 to SF000002000 (S ELE CAP 330U 6.3V M 6.3X5.9 LESR15M VU)	09/07/20	DVT
					and BOM structure to @	09/07/20	DVT
					Cahnge PR226 to SD000009080 (S RES 1/16W 1.91K +-1% 0402)	09/07/20	DVT
					Cahnge PC116 to SGA20331E10 (S POLY C 330U 2V Y D2 LESR9M EEFSX H1.9)	09/07/21	DVT
					Cahnge PC179 to SE026683K80 (S CER CAP .068U 16V K X7R 0603)	09/07/22	DVT
					Cahnge PC53 to SE076473K80 (S CER CAP .047U 16V K X7R 0402)	09/07/22	DVT
					Cahnge PC64 to SE107475M80 (S CER CAP 4.7U 6.3V M X5R 0603 H0.8)	09/07/22	DVT
					Cahnge PC212 to SE107475M80 (S CER CAP 4.7U 6.3V M X5R 0603 H0.8)	09/07/22	DVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	Modify GFX_COREP circuit	design change	0.2	54	Cahnge PC189 to SE000000K80 (S CER CAP 1U 6.3V K X5R 0402)	09/07/22	DVT
25	Modify 1.8V circuit	design change	0.2	50	Add PR170 to SD013000080 (S RES 1/10W 0 +-5% 0603)and BOM structure to @ Change PR109, PR117, PC72, PQ58, PQ59 BOM structure to @	09/07/28	DVT
26	Modify 1.8V circuit	design change	0.2	50	Add PUI7 to SA00003KL00(S IC MP2121DQ-LF-Z QFN 10P PWM) Add PD16 to SC500001I80(S SCH DIO B340A SMA VISHAY) BOM structure to @ Add PR173 to SD034402380(S RES 1/16W 402K +-1% 0402)	09/07/28	DVT
27	Modify 1.8V circuit	design change	0.2	50	Add PR174 to SD034316380(S RES 1/16W 316K +-1% 0402) Add PR171 to SD028000080(S RES 1/16W 0 +-5% 0402)BOM structure to @ Add PRI13 to SD028470280(S RES 1/16W 47K +-5% 0402)	09/07/28	DVT
28	Modify 1.8V circuit	design change	0.2	50	Add PC123,PC124 to SE053106Z80(S CER CAP 10U 10V Z Y5V 0805) Add PC127 to SE076103K80(S CER CAP .01U 16V K X7R 0402) Add PC218, PC219 to SE000000I10(S CER CAP 22UF 6.3V M X5R 0805 H1.25)	09/07/28	DVT
29	Modify 1.8V circuit	design change	0.2	50	Add PR41, PR42 to SD001470B80(S RES 1/4W 4.7+-5% 1206)	09/07/28	DVT
30	Modify 5V/3V circuit	add snubber(PR42 PC36), (PR41 PC35) add boost PR43, PR44	0.2	47	Add PC35, PC36 to SE074681K80(S CER CAP 680P 50V K X7R 0402) Add PR43, PR44 to SD013220B80(S RES 1/10W 2.2 +-5% 0603)	09/07/28	DVT
31	Modify VGA_COREP circuit	add snubber(PR315 PC206) add boost PR311	0.2	52	Add PR311 to SD013220B80(S RES 1/10W 2.2 +-5% 0603)and BOM structure to VGA@ Change PR315 PC206 BOM structure to VGA@	09/07/28	DVT
32	Modify CPU circuit	add snubber(PR220 PC158), (PR252 PC184) add boost PR217, PR249	0.2	55	Add PR220, PR252 to SD011220B80(S RES 1/4W 2.2 +-5% 1206) Add PC158, PC184 to SE074681K80(S CER CAP 680P 50V K X7R 0402) Add PR217, PR249 to SD013220B80(S RES 1/10W 2.2 +-5% 0603)	09/07/28	DVT
33	Modify +1.1VS_VTTP circuit	design change	0.2	53	Cahnge PR141 to SD034787280(S RES 1/16W 78.7K +-1% 0402) Cahnge PR143 to SD034649180(S RES 1/16W 6.49K +-1% 0402)	09/07/28	DVT
34	Modify OTP circuit	design change	0.2	46	Cahnge PH1 to SL200000U00(S THERM_100K +-1% TSMOB104F4251RZ 0402) Cahnge PH2 to SL200000U00(S THERM_100K +-1% TSMOB104F4251RZ 0402)	09/07/28	DVT
35	Modify +1.1VS_VTTP circuit	design change(OCP)	0.2	53	Cahnge PR135 to SD034280180(S RES 1/16W 2.8K +-1% 0402)	09/07/29	DVT
36	Modify GFX_COREP circuit	design change	0.2	54	Cahnge PH3 to SL200000Y00(10K +-5% TSMOA103J4302RE 0402)	09/07/29	DVT
37	Modify CPU circuit	design change	0.2	55	Cahnge PH6 to SL200000W00(10K +-1% TSMOA103F34D1RZ 0402)	09/07/29	DVT
38	Modify 1.5V circuit	Change to 3mm height choke for thermal issue	0.2	51	Cahnge PL7 to SH00000AB00(S COIL 1UH +-20% PCMB103T-1R0MS 13A)	09/08/06	DVT
39	Modify VGA_COREP circuit	design change (GS sample define 1.03V,+1.05VSDGPU Vo=1.05V)	0.3	52	Cahnge PR159 to SD034634180(S RES 1/16W 6.34K +-1% 0402) Cahnge PR167 to SD034365180(S RES 1/16W 3.65K +-1% 0402)	09/08/24	PVT
40	Modify 1.8V circuit	design change	0.3	50	Cahnge PC127 to SE076104K80(S CER CAP .1U 16V K X7R 0402)	09/08/24	PVT
41	Modify chager circuit	design change	0.3	48	Cahnge PR88 to SD034154280(S RES 1/16W 15.4K +-1% 0402) Change PR81 to SD034154380(S RES 1/16W 154K +-1% 0402)	09/08/26	PVT
42	Modify VGA_COREP circuit	design change	0.3	52	Change PR160 BOM structure to VGA@ VID pull high voltage change to +3VS_DELAY	09/09/03	PVT
43	Modify +1.1VS_VTTP circuit	design change	0.3	53	Change PR130 BOM structure to @	09/09/03	PVT
44	Modify 0.75V circuit	design change	0.3	50	Cahnge PR120 to SD034280180(S RES 1/16W 2.8K +-1% 0402)	09/09/11	PVT
45	Modify VGA_COREP circuit	design change	0.3	52	Cahnge PR316 to SD034300280(S RES 1/16W 30K +-1% 0402) Change PR164 BOM structure to @	09/09/11	PVT
46	Modify +1.1VS_VTTP circuit	design change	0.3	53	Cahnge PR135 to SD034205180(S RES 1/16W 2.05K +-1% 0402)		

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
47	Modify OTP circuit	design change	0.3	46	Change PR23 to SD00000AJ80(S RES 1/16W 12.4K +-1% 0402) Change PR26 to SD034158280(S RES 1/16W 15.8K +-1% 0402)	09/09/14	PVT
48	Modify 1.8V circuit	design change	0.3	50	Change PL6 to SH000009Q00(S COIL 2.2UH 20% MSCDRI-74A-2R2M-E 6.5A)	09/09/16	PVT
49	Modify 5V/3V circuit	design change	0.3	47	Change PU4 to SA00001TN00(S IC ISL6237IRZ-T QFN 32P)	09/09/16	PVT
50	Modify 0.75V circuit	design change	0.3	50	Change PR120 to SD00000AJ80(S RES 1/16W 12.4K +-1% 0402)	09/10/08	PVT
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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1				4	R72 bom structure	7/23	0.2
2				5	reserve R735	7/23	0.2
3				8	rename CPU VDDQ from +1.5V to +1.5V_CPU	7/23	0.2
4				8	R146 BOM structure	7/23	0.2
5				11	reserve S3 power consumptiosn circuit	7/23	0.2
6				12	change Y1 Y4 Y6 footprint	7/23	0.2
7				13	add ME_EN# from EC to PCH	7/23	0.2
8				14	pop Y6,C254,C255 , and project ID pin	7/23	0.2
9				17	change USB port 8 to port 1 , port 2 to port 8	7/23	0.2
10				18	GPIO35 pin(VGa presetnt) modfiy	7/23	0.2
11				19	R605 and R628 BOM structure modify	7/23	0.2
12				22	add VGA thermal sensor from EC to VGA	7/23	0.2
13				23	pop R479,del R491	7/23	0.2
14				29	L29~L34 change from 0805 to 0603	7/23	0.2
15				30	Q45,Q47 gate voltage change from +3VS to +3VS_delay	7/23	0.2
16				37	change R306 to 8.2K, add D29, rename EC_MUTE	7/23	0.2
17				38	Jfun1 pin3 change form KSO1 to KSO3	7/23	0.2
18				39	del SW2	7/23	0.2
19				41	change R333, R336 to 39k,15k, add R681,C707	7/23	0.2
20				43	reserve Q58,Q59,R728,R326, change U26,R688	7/23	0.2
21				24	reserve C710	7/23	0.2
22				28	reserve U44,U45	7/23	0.2
23				19	update L7,L8,L10,L11 footprint	7/23	0.2

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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1				30	pop R248, R271,R265	7/23	0.2
2				7	pop C165, del C170	7/23	0.2
3				18	unpop R532, R86	7/23	0.2
4				5	add R472 and C713	8/31	0.3
5				11	add C714	8/31	0.3
6				12	add C715	8/31	0.3
7				17	USB20 port 6 change to USB20 port 9	8/31	0.3
8				24	3VS_delay related circuit	8/31	0.3
9				30	del R236,C257 , pop R254,C268 in all sku	8/31	0.3
10				33	unpop R3 , U1, pop R6 , change R306 to 18K	8/31	0.3
11				37	ME_EN change from U25,75 to U25.16	8/31	0.3
12				29	pop Q6,Q7 in all sku	8/31	0.3
13				29	change L29~L34 footprint	8/31	0.3
14				41	del D25,D26,D27	8/31	0.3
15				43	update C705,C706 BOM structure	8/31	0.3
16				14	unpop R112	8/31	0.3
17				7	change C165 p/n	8/31	0.3
18				40	pop C353	9/10	0.3
19					change R157,R527,R570,R575,R582,R634,R239,R64 to 0 ohm		0.3
20				5	add R746,R747	9/10	0.3
21				12	U27 clk gen change to siligo	9/10	0.3
22				40	del C371,C372	9/10	0.3
23				3	Modify BOM Config add S3@ on all SKU	10/20	1.0

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1				14	Change R209,C254,C255,Y6 BOM config to UMA@	10/20	1.0
2				19	Added C257	10/20	1.0
3				22	Change N11 to A2 (P/N SA00003HZ10)	10/20	1.0
4				22	Added R748 and R749 as I2C pull high resistor.	10/20	1.0
5				22	Pop R36,R37 as DIS@	10/20	1.0
6				28	Change Q11,Q19 BOM config to SG@	10/20	1.0
7				28	Change R502,R484 BOM config to DIS only@	10/20	1.0
8				37	Change R306 to 33k(Board ID)	10/20	1.0
9				38	Change LED9 PN to SC5191UD00	10/20	1.0
10				43	Change R296 to 47K,R295 to 470	10/20	1.0
11				44	Change LED Resistors:	10/20	1.0
12					R373 to 243,R381 and R383 to 100,R377 to 243,		
13					R375 and R376 to 470,R349 to 100,R350 to 191		
14					R304 to 499		1.0
15				17	Change C256 to 22u	10/22	
16				18	ADD R750 10K pull hig resistor	10/22	1.0
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